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## 1.1 COMPUTER OVERVIEWS

### 1.1.1 Introduction

Figure 1.1-1

The basic purpose of the PTS 6000 System is to provide computerized terminals for the work positions in bank- and post offices etc. This requires, besides special equipment at each work position, a Terminal Computer which controls the transactions carried out and which either stores the transaction data (off-line systems) or transfers it via modems and telephone lines to a remote data centre (on-line systems).

Smaller offices, with 1-4 work positions, can share the computer with a bigger office. The work positions of the smaller office are then connected to the bigger office's computer in a way similar to the on-line connection, i.e. via modems and telephone lines. Such work positions are known as Remote Work Stations whilst the work positions at the computer site are known as Local Work Stations.

In certain cases, mainly when data exchange with other systems is required, it can be necessary to connect peripheral equipment (Magnetic Tape Unit, Disc Unit, Line Printer etc.) to the Terminal Computer.

This manual contains field service information for the Terminal Computers 6811 (also called 6810), 6812-6814 and 6824.

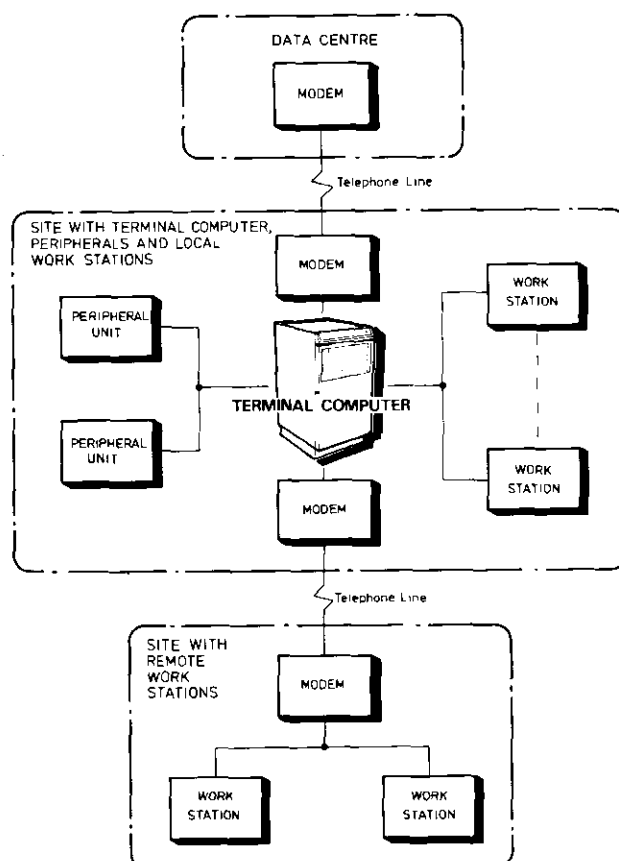


Figure 1.1-1 Basic System Configuration

### Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B, 1C) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; one or two digital cassette recorders for program load and back-up, a control panel, a power supply unit and a cooling fan.

### Processing Units & Memory System

The computer is based on a central processing unit (CPU) of type P852. An optional I/O processor (IOP 6827) can be added to increase the capacity of data transfers when heavy traffic is expected between memory and interface units along the GP bus.

The memory capacity is 8-32K 16-bit words, built to the desired range by plugging in one or two core memory modules. Two different modules are available; CMM 6822 with a capacity of 8K, and CMM 6823 with a capacity of 16K.

#### NOTE

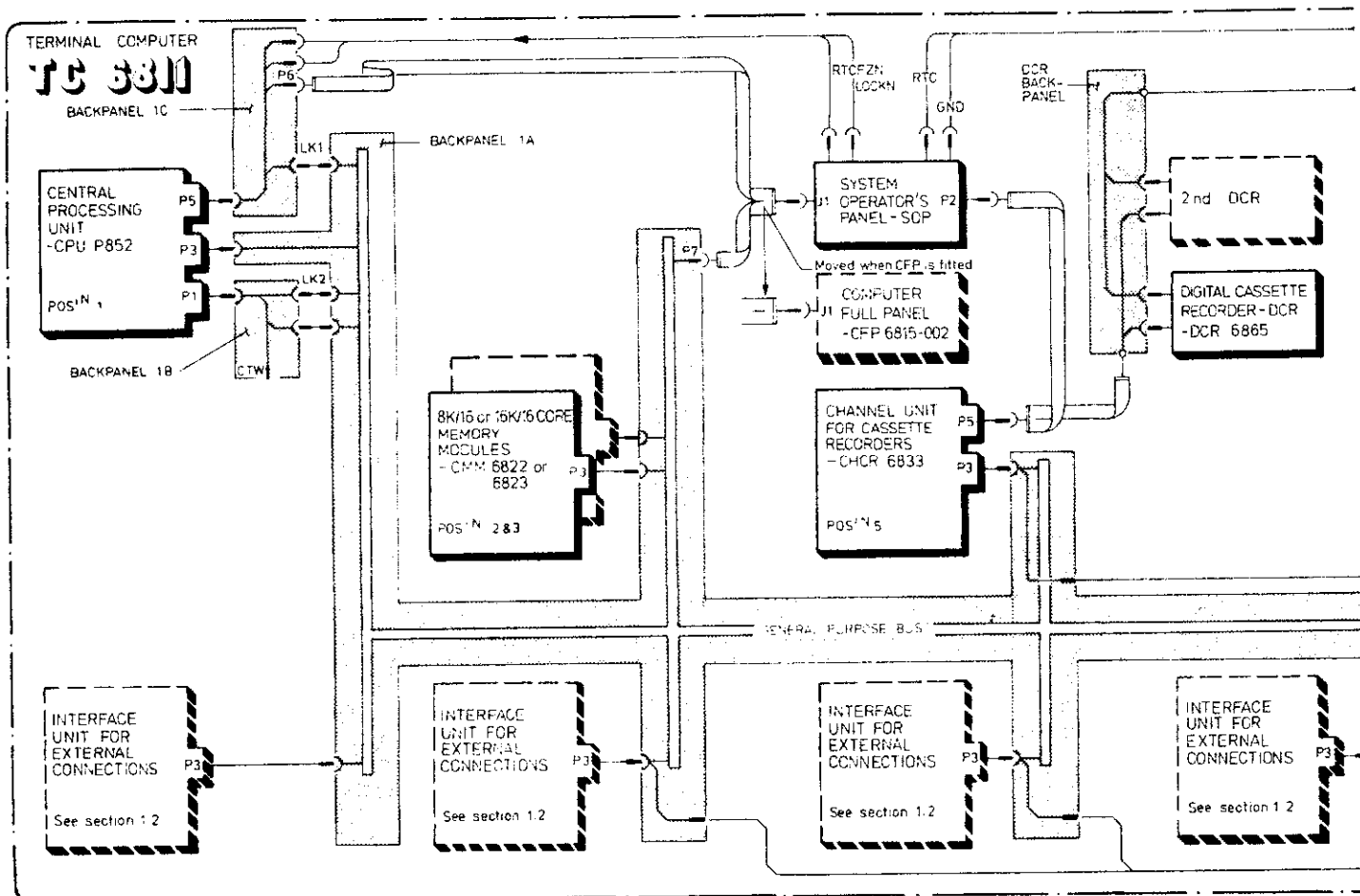
Some of the 6810/11 computers have been upgraded according to a modification kit known as UK01. These computers are using a CPU of type P857, two CMMs of type 6825 (each of 32K 16-bit words) and a memory management unit, MMU 6828. Processing and memory capacity has then been increased to the class of the TC 6813.

### Program Load & Back-Up Medium

The cabinet is able to house up to two digital cassette recorders of type 6865 (6861 in earlier computer models). These recorders are controlled via the bus-connected interface unit CHCR 6833.

### Control Panels

A system operator's panel (SOP) is always fitted to the computer. This panel provides the control and display facilities that are required for the daily routines and operates via the CHCR 6833. When extended control and display facilities are required, it is possible to add a computer full panel (CFP 6815-002).



## External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre, are described in section 1.2; EXTERNAL CONNECTIONS.

## Power Supply

The power supply unit (PSU) is available in two basic versions; one for mains sources of 100-127V/60Hz and another one for 200-240V/50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN) and a system reset signal (RSLN).

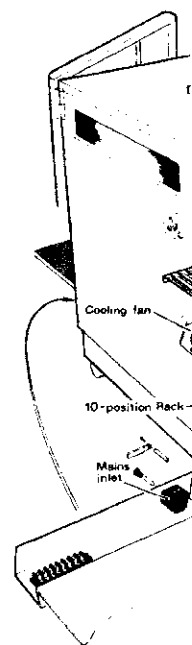
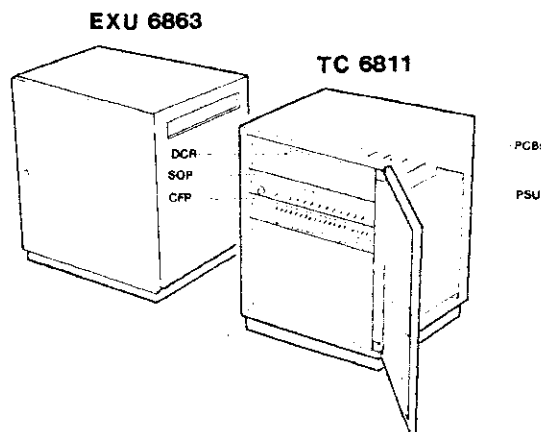
## Extension Unit

Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6863. This is a stripped computer cabinet where the rack with backpanel 1A and the PSU have been retained.

The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to an IOP in the TC cabinet. Such lines are in both cabinets terminated on wire wrap posts close to the extension plugs on backpanel 1A.

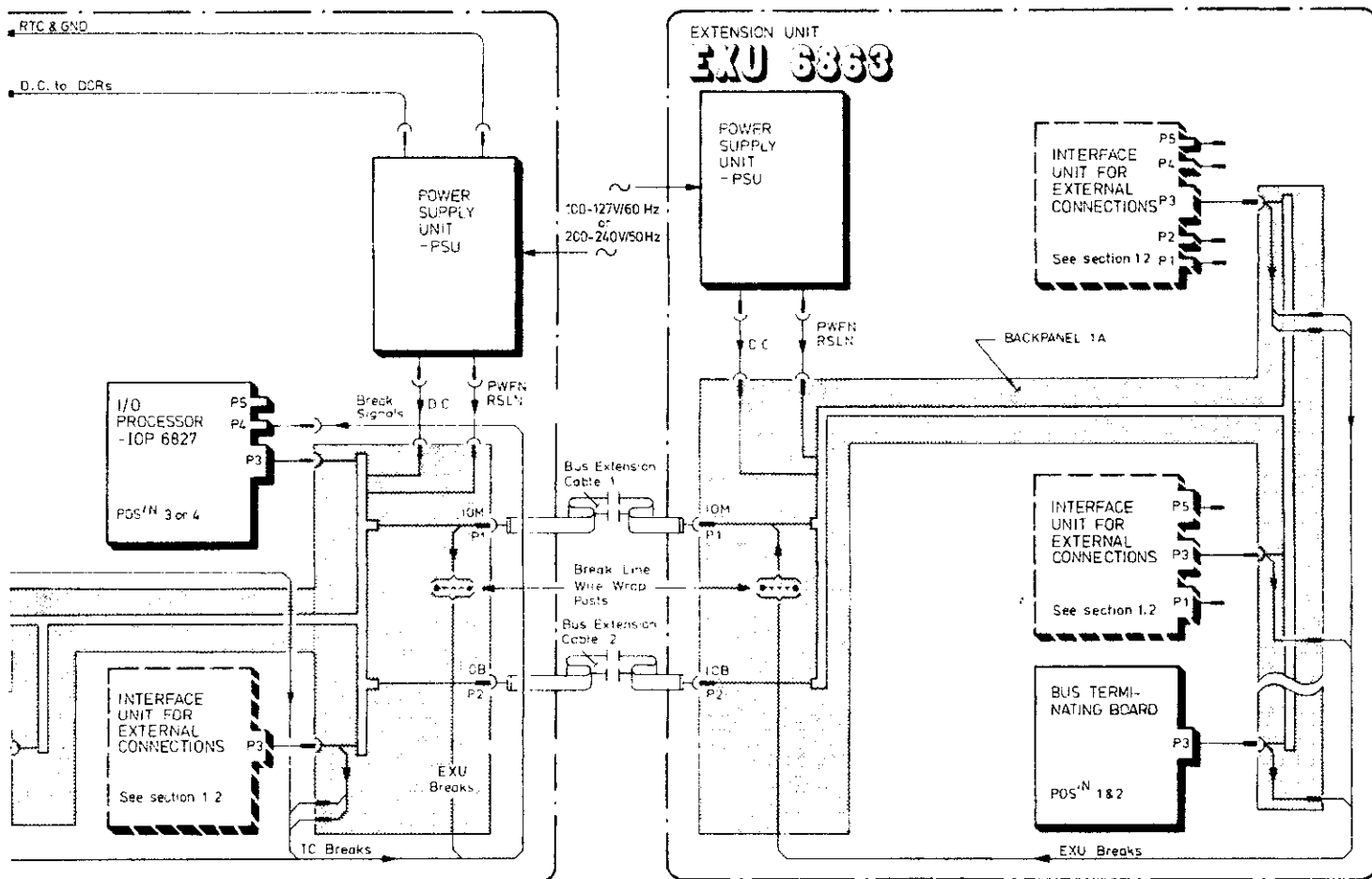
The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.

A limited outfit in the extension cabinet and limitations in the extended bus lead to some restrictions. The following computer sub-modules can NOT be placed in an extension unit; CPU, IOP, CMM, MMU and CHCR.









TC & EXU CABINETS — Front view of backpanels and connectors

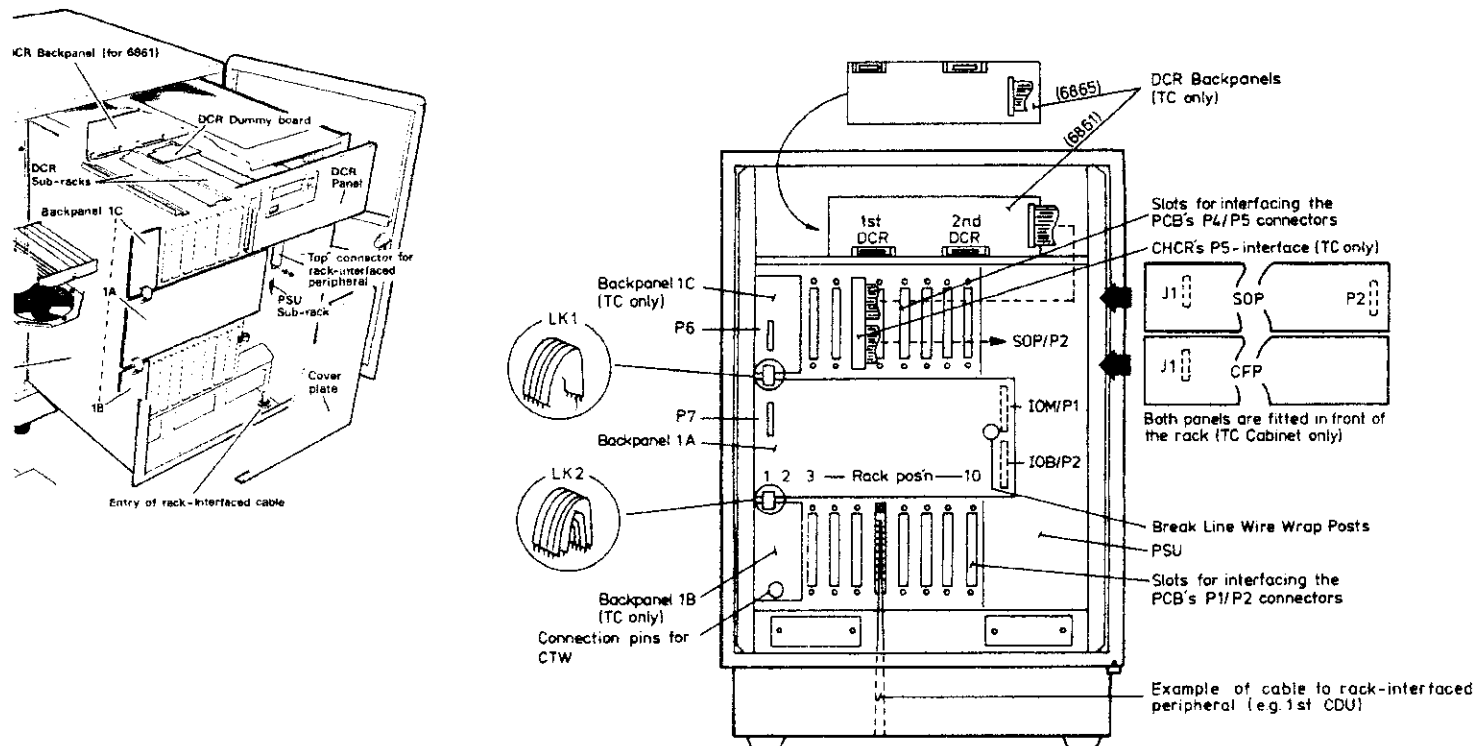


Figure 1.1-2 TC 6811/EXU 6863 - Basic Configuration



## SUBNUMBER LIST

Subnumber	Description (main characteristics)	Comments
001	220/200–240 V, 50 Hz, DCR 1 (CPU P852)	Replaced by 6811–301 in the beginning of 1979.
101	100–127 V, 60 Hz, DCR 3, UL/CSA (CPU P852)	
102	= 101 excl. DCR unit	Special version.
201	220/200–240 V, 50 Hz, DCR 1 + UK01 (CPU P857)	Arise only in field. UK01 = Upgrading Kit 6810–601
301	200–240 V, 50 Hz, DCR 3 (CPU P852)	Present standard version. Replaces 6811–001.
401	200–240 V, 50 Hz, DCR 3 + UK01 (CPU P857) excl. CMM	6811–301 excl. CPU P852 and CMM, modified with Upgrading Kit 6810–601 UK01.
402	100–127 V, 60 Hz, DCR 3, UL/CSA + UK01 (CPU P857) excl. CMM	6811–101 excl. CPU P852 and CMM, modified with Upgrading Kit 6810–601 UK01.
501	200–240 V, 50 Hz, DCR 3 excl. CPU and CMM	Special version of 6811–301.

DCR 1 = PTS 6861 DCR

DCR 3 = PTS 6865 DCR



**Physical Structure**

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B, 1C, 1D) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; program load and back-up media (cassette recorders and/or flexible disc drives), a control panel, a power supply unit and a cooling fan.

**Processing Units & Memory System**

The computer is based on a central processing unit (CPU) of type P852. An optional I/O processor (IOP 6827) can be added to increase the capacity of data transfers when heavy traffic is expected between memory and interface units along the GP bus.

The memory capacity is fixed to 32K 16-bit words by a single core memory module, CMM 6825.

**Program Load & Back-Up Media**

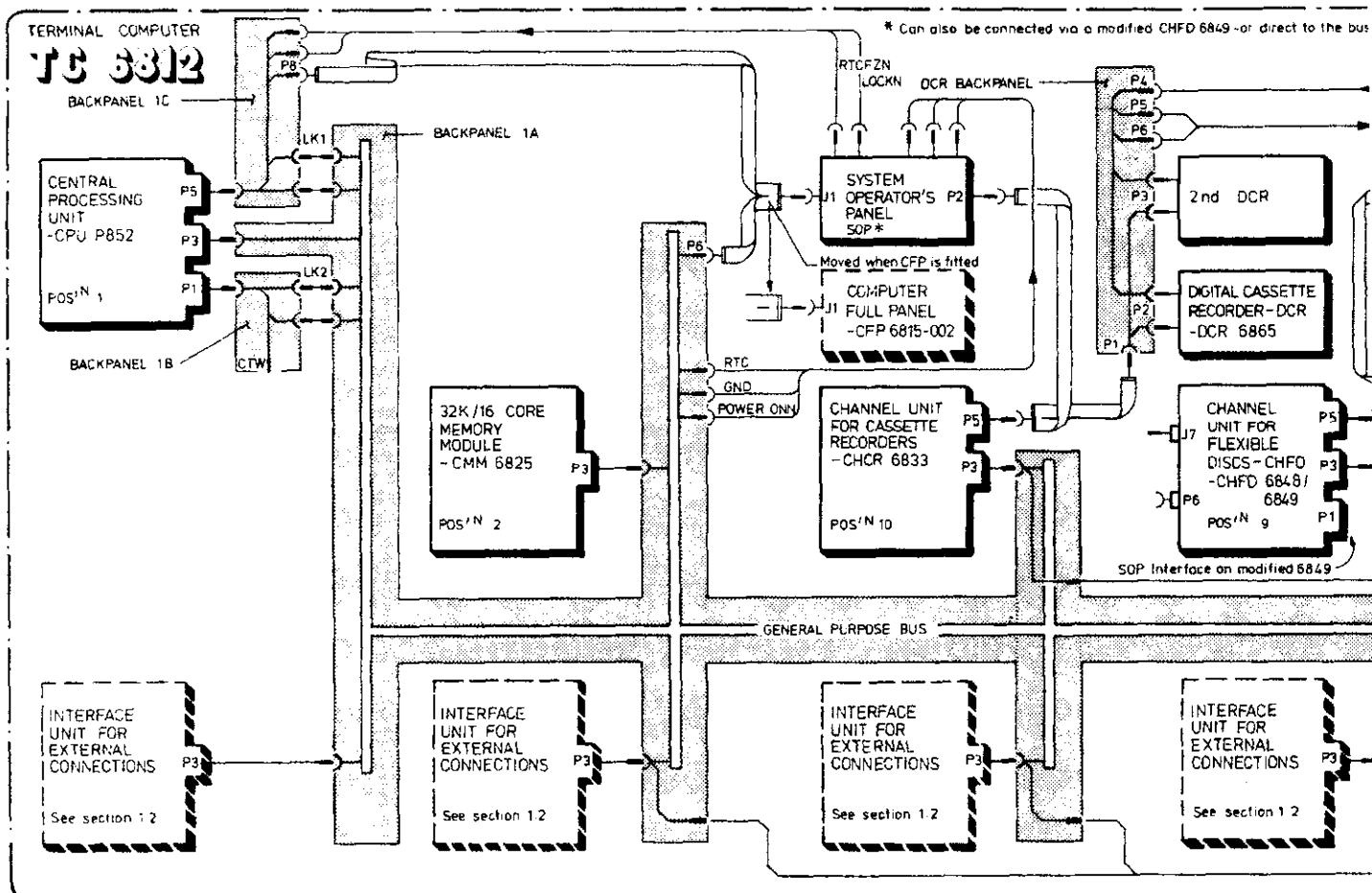
The cabinet is able to house up to two digital cassette recorders, DCR 6865, and up to two flexible disc drives, FDD 6867 (250 Kbytes) or FDD 6791 (1 Mbyte). The recorders are controlled via the busconnected interface unit CHCR 6833, and the flexible disc drives via CHFD 6848 (for FDD 6867) or CHFD 6849 (for FDD 6791).

**Control Panels**

A system operator's panel (SOP), that provides the control and display facilities required for the daily routines, is always fitted to the computer. This panel can be connected in three different ways; via the CHCR 6833 as shown in figure, via a modified CHFD 6849 (in both cases a 'passive' SOP), or direct to the backpanel ('active' SOP, modified according to an upgrading kit to get an integrated interface logic, CUSOP).

When extended control and display facilities are required, it is possible to add a computer full panel (CFP 6815-002). However, this cabinet is not prepared for any permanent use of this panel (the size of cover plates adapted to the extended full panel, EFP, used in TC 6813).





## External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre, are described in section 1.2; EXTERNAL CONNECTIONS.

## Power Supply

The power supply unit (PSU) can be adapted to either of the mains sources; 100-127V/60Hz, or 200-240V /50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN), a system reset signal (RSLN) and a power on indication (POWER ONN).

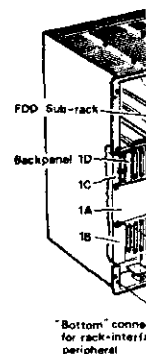
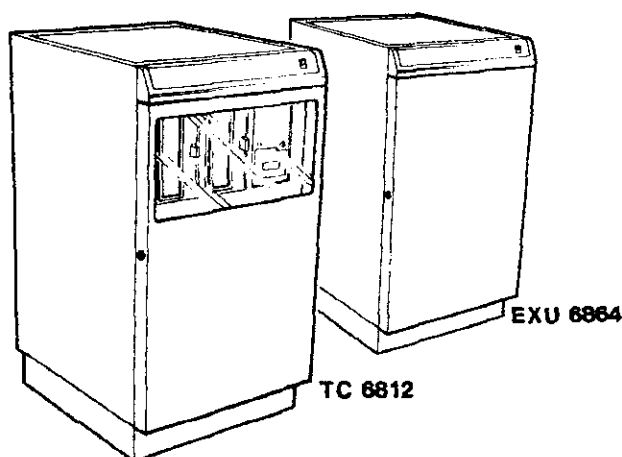
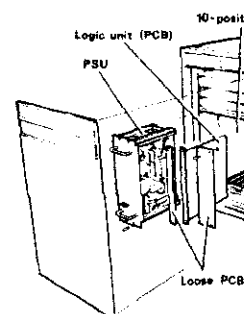
## Extension Unit

Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6864. This is a stripped computer cabinet where the rack with backpanel 1A and the PSU have been retained.

The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to an IOP in the TC cabinet. Such lines are in both cabinets terminated on wire wrap posts close to the extension plugs on backpanel 1A.

The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.

**NOTE**  
When required it is also possible to add a second EXU 6864. The extension cables are then further extended from the cable interface in the first EXU.











## SUBNUMBER LIST

Subnumber			Configuration of back-up / progr. loading media  FDD / DCR / CHFD		
Mains connection					
European 200–240 V 50 Hz	UL/CSA 100–130 V 60 Hz      200–240 V 60 Hz				
001	101	201	1 FDD		CHFD
002	102	202		1 DCR	
003	103	203	1 FDD	1 DCR	CHFD
004	104	204	2 FDD		CHFD
005	105	205		2 DCR	
006	106	206	2 FDD	1 DCR	CHFD
007	107	207	1 FDD	2 DCR	CHFD

Special versions receive subnumbers starting with 5 = 6812 – 5XX

Subnumber	
501–507	Equal to 001–007 excl. CMM



### Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B, 1C, 1D) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; program load and back-up media (cassette recorders and/or flexible disc drives), a control panel, a power supply unit and a cooling fan.

### Processing Units & Memory System

The computer is based on a central processing unit (CPU) of type P857. One or two optional I/O processors (IOP 6827) can be added to increase the capacity of data transfers when heavy traffic is expected between memory and interface units along the GP bus.

The memory capacity is 32-128K 16-bit words, built to the desired range by plugging in 1-4 core memory modules of type 6825 (each of 32K). When more than one CMM are fitted, the computer must also be equipped with a memory management unit, MMU 6828.

### Program Load & Back-Up Media

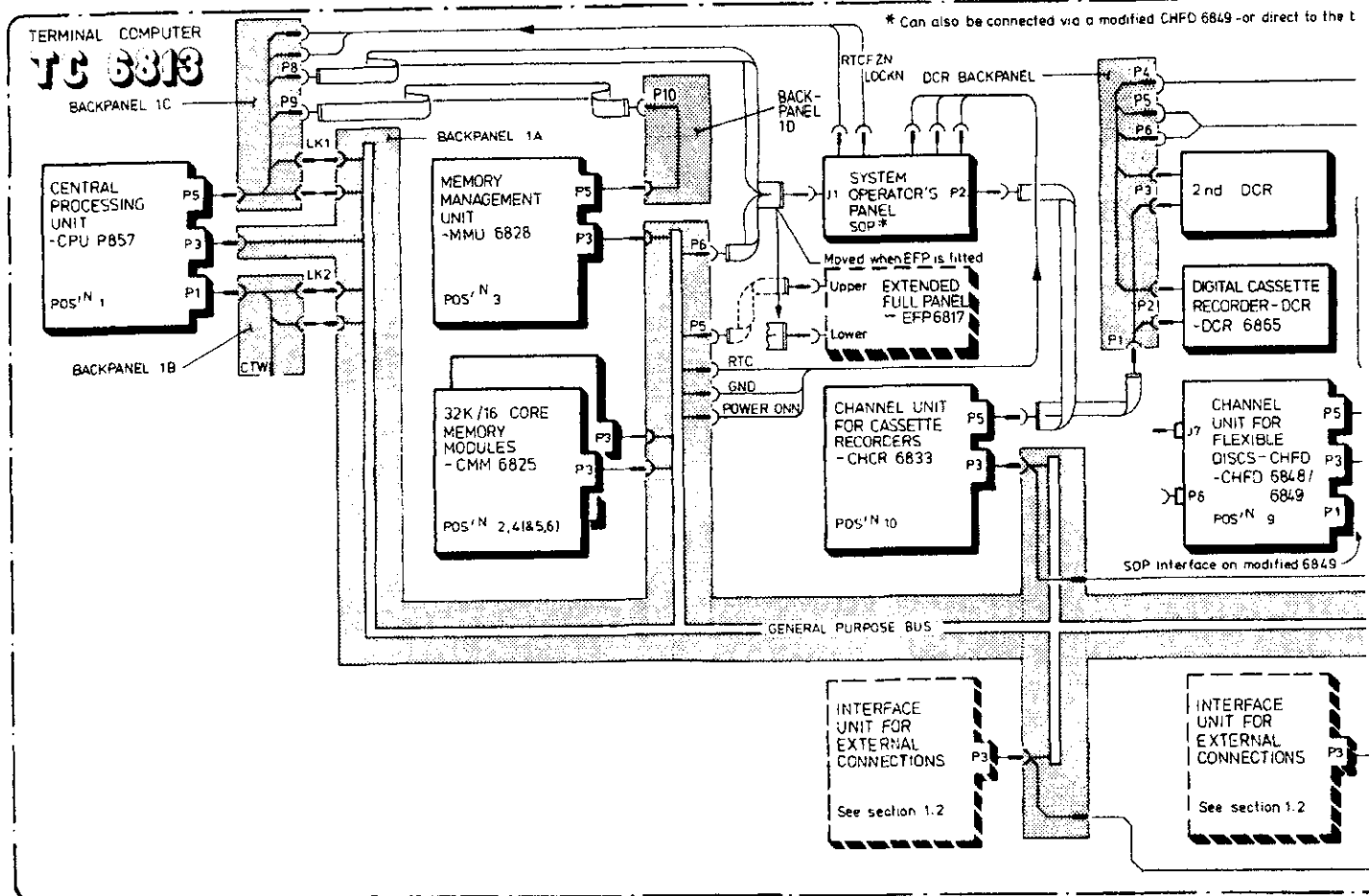
The cabinet is able to house up to two digital cassette recorders, DCR 6865, and up to two flexible disc drives, FDD 6867 (250 Kbytes) or FDD 6791 (1 Mbyte). The recorders are controlled via the busconnected interface unit CHCR 6833, and the flexible disc drives via CHFD 6848 (for FDD 6867) or CHFD 6849 (for FDD 6791).

### Control Panels

A system operator's panel (SOP), that provides the control and display facilities required for the daily routines, is always fitted to the computer. This panel can be connected in three different ways; via the CHCR 6833 as shown in figure, via a modified CHFD 6849 (in both cases a 'passive' SOP), or direct to the backpanel ('active' SOP, modified according to an upgrading kit to get an integrated interface logic, CUSOP).

When extended control and display facilities are required, it is possible to add an extended full panel (EFP 6817) in addition to the SOP.





### External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre, are described in section 1.2; EXTERNAL CONNECTIONS.

### Power Supply

The power supply unit (PSU) can be adapted to either of the mains sources; 100-127V/60Hz, or 200-240V /50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN), a system reset signal (RSLN) and a power on indication (POWER ONN).

### Extension Unit

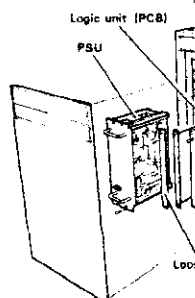
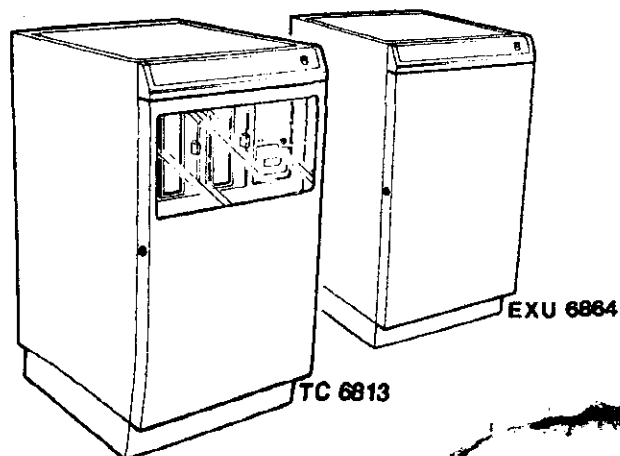
Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6864. This is a stripped computer cabinet where the rack with backpanel 1A and the PSU have been retained.

The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to an IOP in the TC cabinet. Such lines are in both cabinets terminated on wire wrap posts close to the extension plugs on backpanel 1A.

The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.

#### NOTE

When required it is also possible to add a second EXU 6864. The extension cables are then further extended from the cable interface in the first EXU.



FDD Sub-rack.

Backpanel 1D -

1C -

1A -

1B -

"Bottom" for rack periphery









## SUBNUMBER LIST

PTS 6813

TC

## I TC 6813 basic unit incl. PSU, SOP, CPU

Subnumber			Cabinet version
Mains connection			
200–240 V 50 Hz Euro-plug	100–130 V 60 Hz US-plug	200–240 V 60 Hz US-plug	
			Cabinet prepared for
011	111	211	1 (or 1/4) MB FDD + DCR
012	112	212	1 (or 1/4) MB FDD (NO DCR)
013	113	213	1/4 MB FDD + DCR

## II TC 6813 basic unit incl. PSU, SOP, CPU, CMM 6825, MMU 6828, CHCR 6833, CHLT 6831

Subnumber			Configuration of back-up and progr. loading media  FDD / DCR / CHFD		
Mains connection					
200–240 V 50 Hz Euro-plug	100–130 V 60 Hz US-plug	200–240 V 60 Hz US-plug			
001	101	201	1 FDD		CHFD
002	102	202		1 DCR	
003	103	203	1 FDD	1 DCR	CHFD
004	104	204	2 FDD		CHFD
005	105	205		2 DCR	
006	106	206	2 FDD	1 DCR	CHFD
007	107	207	1 FDD	2 DCR	CHFD
	108				CHFD
501–507			Equal to 001–007 excl. CMM		
551			Special version for the Hugin-project		



### Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B and 1C) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; one or two flexible disc drives, a control panel, a power supply unit and a cooling fan.

### Processing Unit & Memory System

The computer is based on a central processing unit (CPU) of type P857R or P857RA. This CPU also includes an I/O processor and a memory management unit. The integrated IOP function has a capacity equal to two IOPs of type 6827, and the memory management is able to address 1Mbyte.

The memory capacity is 32-128K 16-bit words, built to the desired range by plugging in 1-4 core memory modules of type 6825 (each of 32K).

### Program Load & Back-Up Media

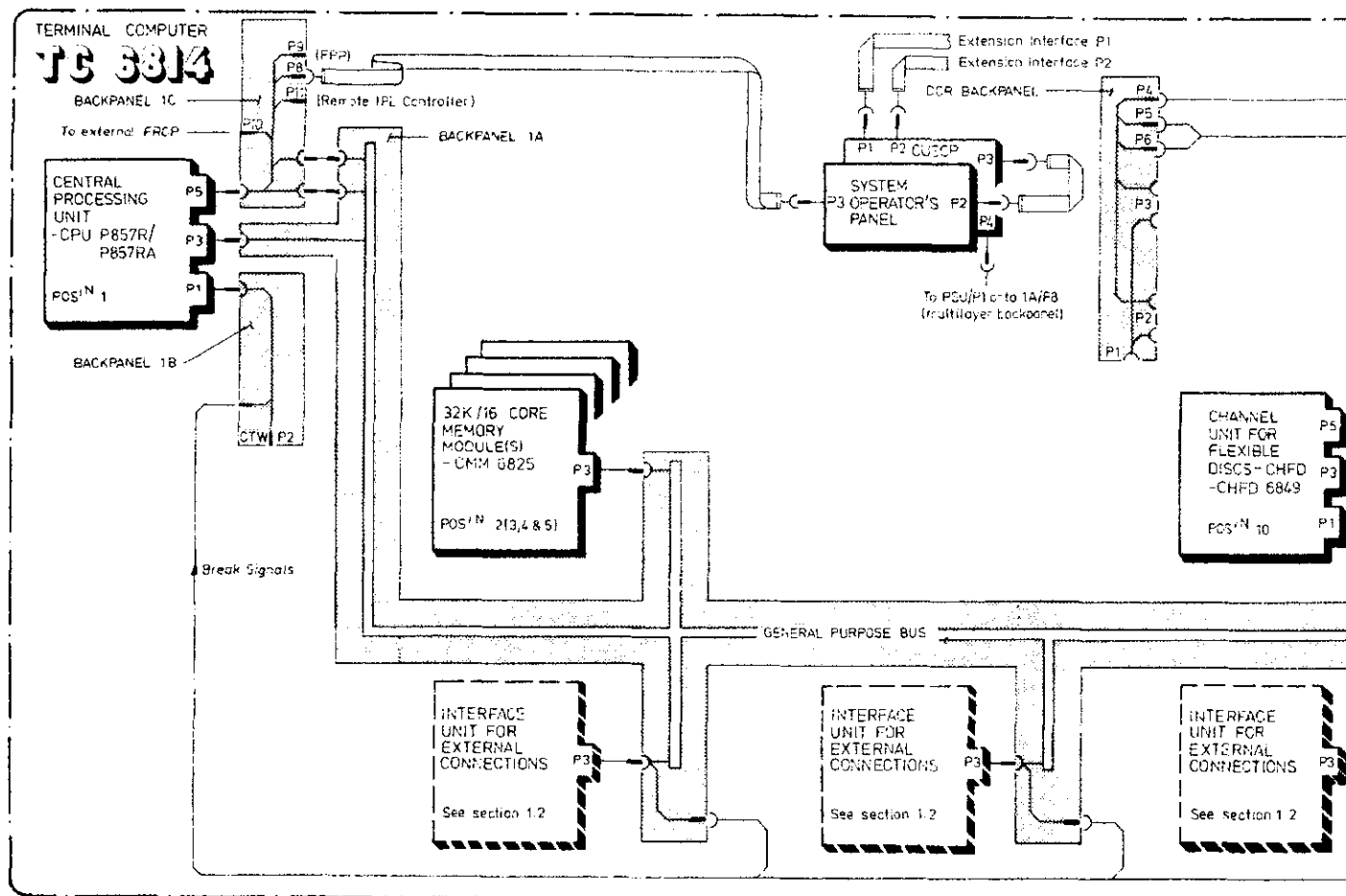
The cabinet is able to house up to two flexible disc drives, FDD 6791 (1Mbyte). The drives are controlled via the busconnected interface unit CHFD 6849. However, if desired, the cabinet can instead be equipped with drives of type FDD 6867 (250 Kbyte) and a controller of type CHFD 6848. It is even possible to install up to two digital cassette recorders (DCR 6865) with necessary controller, CHCR 6833.

### Control Panels

A system operator's panel (SOP), that provides the control and display facilities required for the daily routines, is always fitted to the computer. This panel has now got an integrated interface unit (Control Unit SOP, CUSOP) that makes it independent of other units like CHCR and CHFD.

When extended control and display facilities are required, it is possible to connect an external Full Refreshed Control Panel, FRCP 6981.

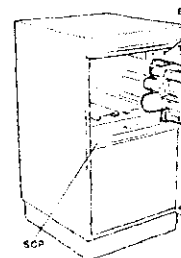




## External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre, are described in section 1.2: EXTERNAL CONNECTIONS.

The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.



## Power Supply

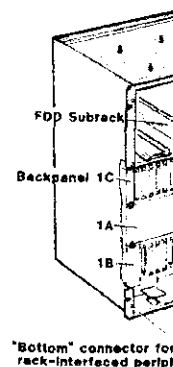
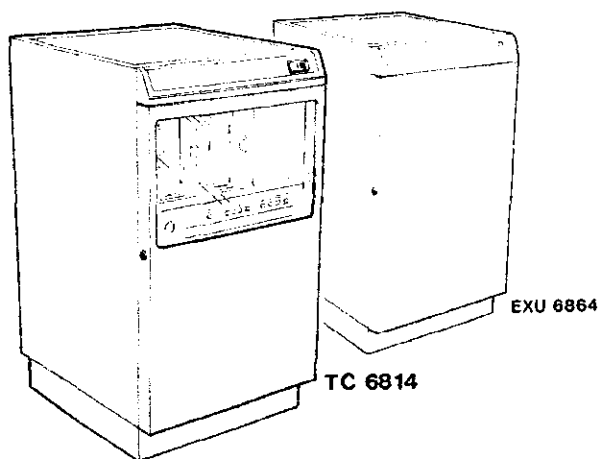
The power supply unit (PSU) can be adapted to either of the mains sources: 100-127V/60Hz, or 200-240V /50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN), a system reset signal (RSLN) and a power on indication (POWER ONN).

NOTE  
When required it is also possible to add a second EXU 68b4. The extension cables are then further extended from the cable interface in the first EXU.

## Extension Unit

Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 68b4. This is a stripped computer cabinet where the rack with backpanel 1A and the PSU have been retained.

The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to the CPU in the TC cabinet. Such lines are in both cabinets terminated on extension posts close to the extension plugs on backpanel 1A.







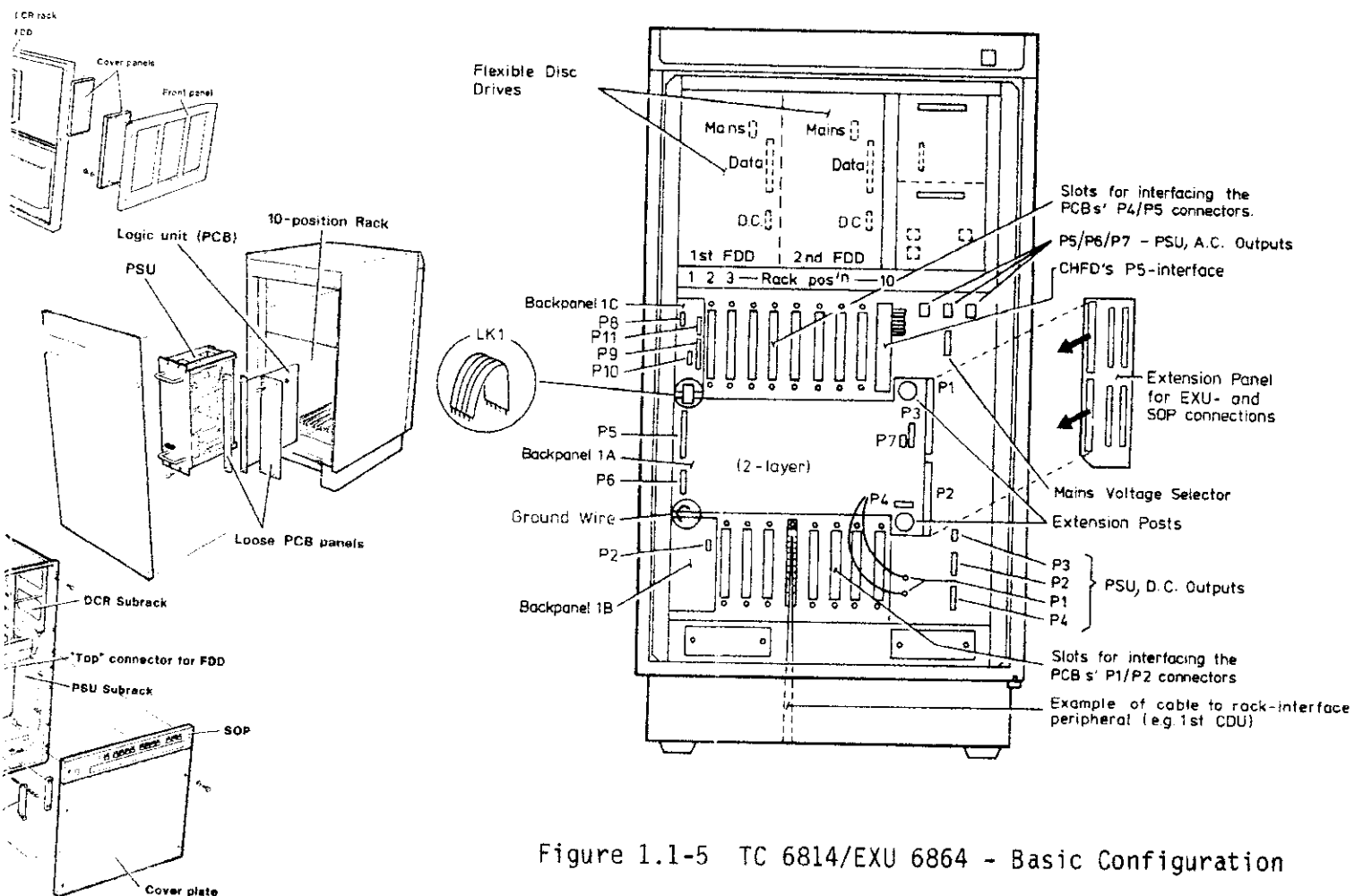
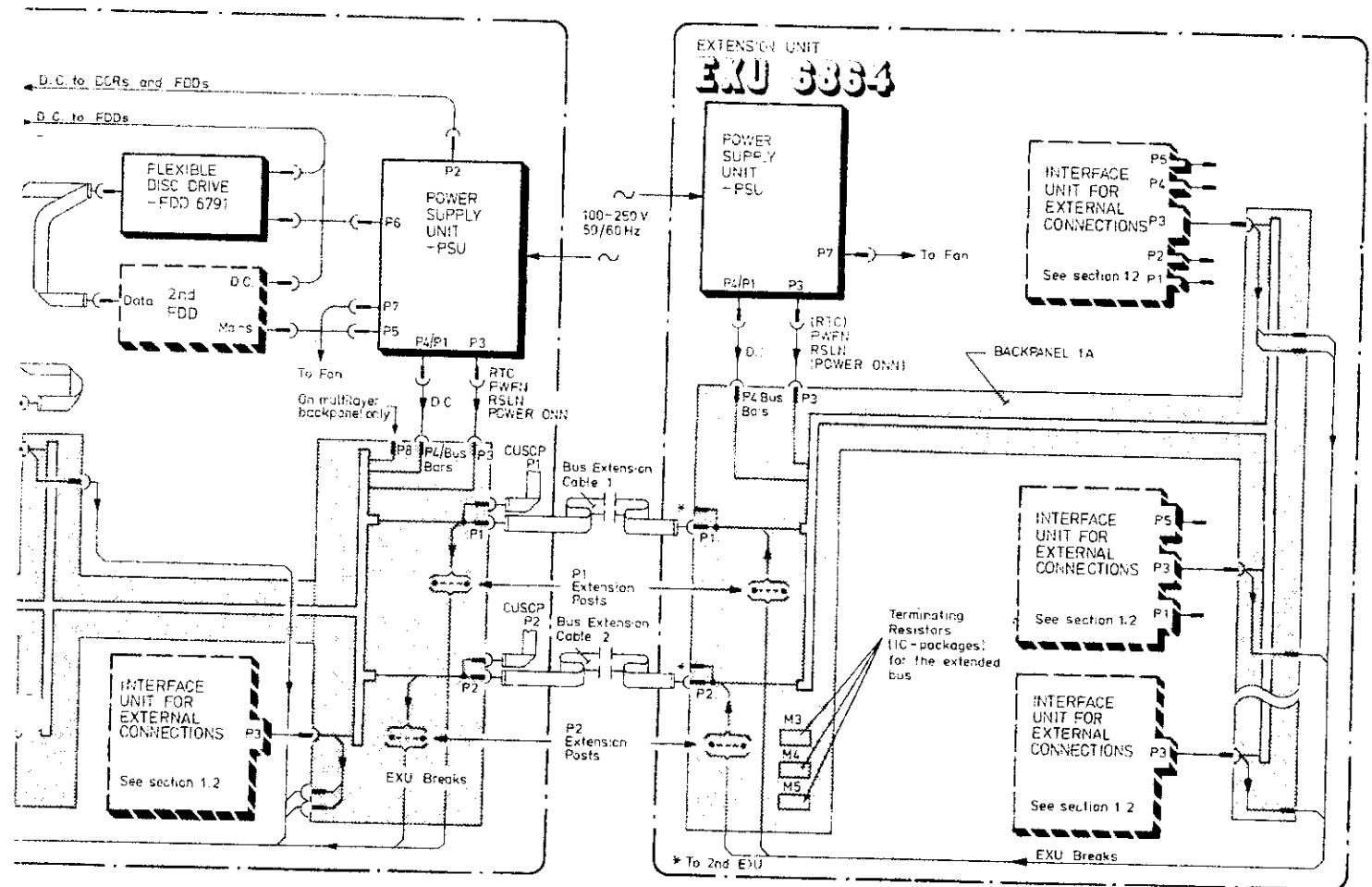


Figure 1.1-5 TC 6814/EXU 6864 - Basic Configuration







### Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B and 1C) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; one or two flexible disc drives, a control panel, a power supply unit with battery back-up, and finally a cooling fan. The cooling system is here of a new type where the air enters and leaves the cabinet via the extended back section.

### Processing Unit & Memory System

The computer is based on a central processing unit (CPU) of type P857RA. This CPU also includes an I/O processor and a memory management unit. The integrated IOP function has a capacity equal to two IOPs of type 6827, and the memory management is able to address 1Mbyte.

The memory capacity is 128-512K 16-bit words, built to the desired range by plugging in 1-4 semiconductor memory modules of type 6781 (each of 128K). The battery back-up provided is capable of maintaining a maximum memory configuration for at least 0.6 hours.

### Program Load & Back-Up Media

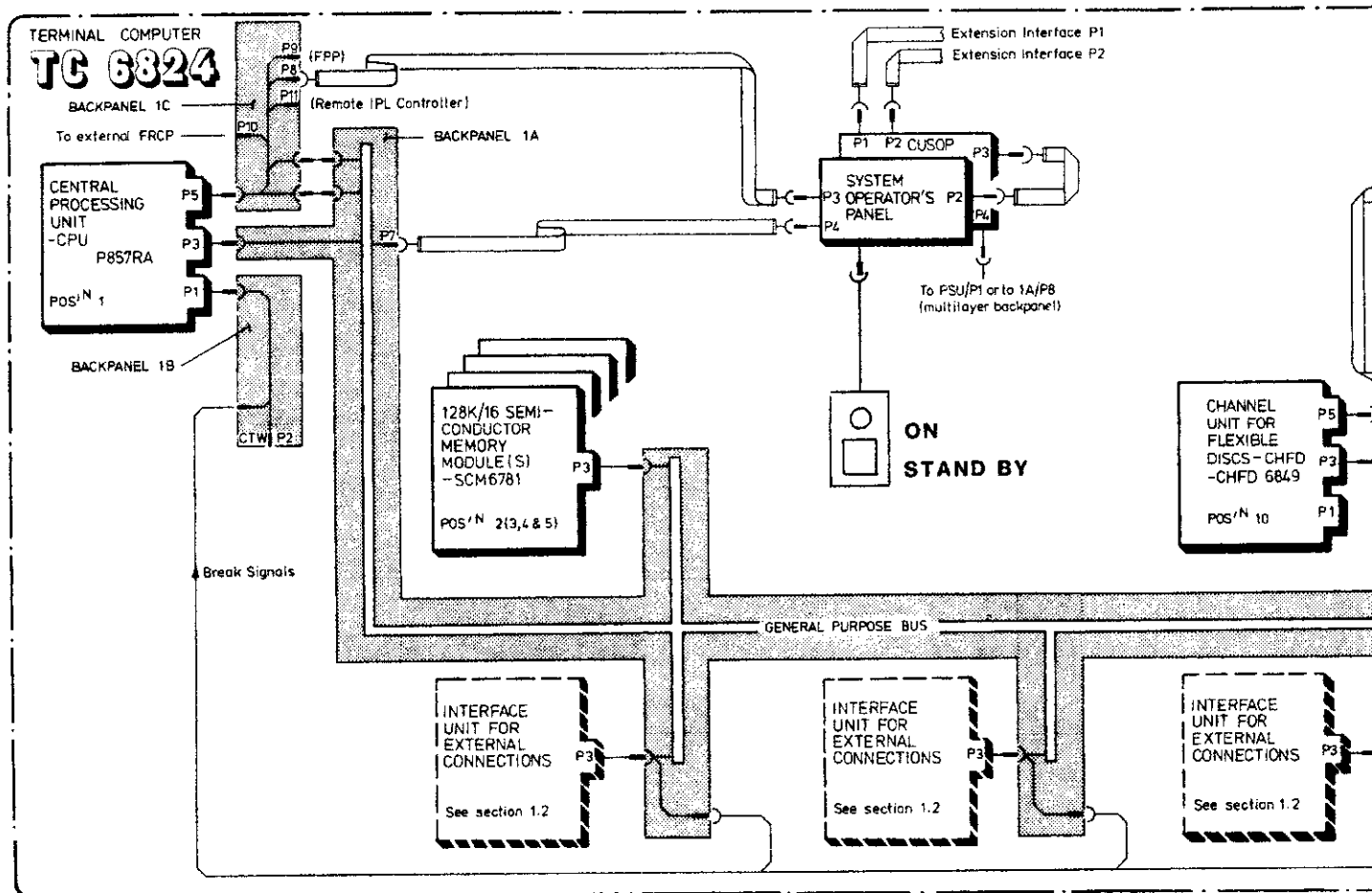
The cabinet is able to house up to two flexible disc drives, FDD 6791 (1Mbyte). The drives are controlled via the busconnected interface unit CHFD 6849. However, if desired, the cabinet can instead be equipped with drives of type FDD 6867 (250 Kbyte) and a controller of type CHFD 6848.

### Control Panels

A system operator's panel (SOP), that provides the control and display facilities required for the daily routines, is always fitted to the computer. This panel has an integrated interface unit (Control Unit SOP, CUSOP) that makes it independent of other units like CHCR and CHFD.

When extended control and display facilities are required, it is possible to connect an external Full Refreshed Control Panel, FRCP 6981.





## External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre are described in section 1.2; EXTERNAL CONNECTIONS.

## Power Supply

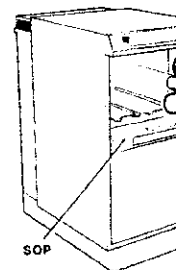
The power supply unit (PSU) can be adapted to either of the mains sources; 100-127V/60Hz, or 200-240V /50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN), a system reset signal (RSLN) and a power on indication (POWER ONN). Battery back-up is provided for the semiconductor memory system. For maximum memory configuration the back-up time is more than 0.6 hours.

## Extension Unit

Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6864. This is a stripped computer cabinet of type 6812/13/14 where the rack with backpanel 1A and the PSU have been retained.

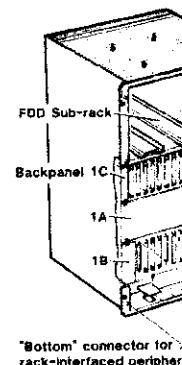
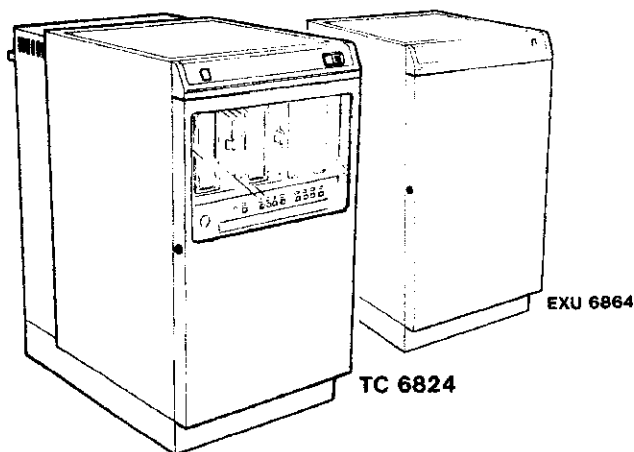
The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to the CPU in the TC cabinet. Such lines are in both cabinets terminated on extension posts close to the extension plugs on backpanel 1A.

The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.



### NOTE

When required it is also possible to add a second EXU 6864. The extension cables are then further extended from the cable interface in the first EXU.







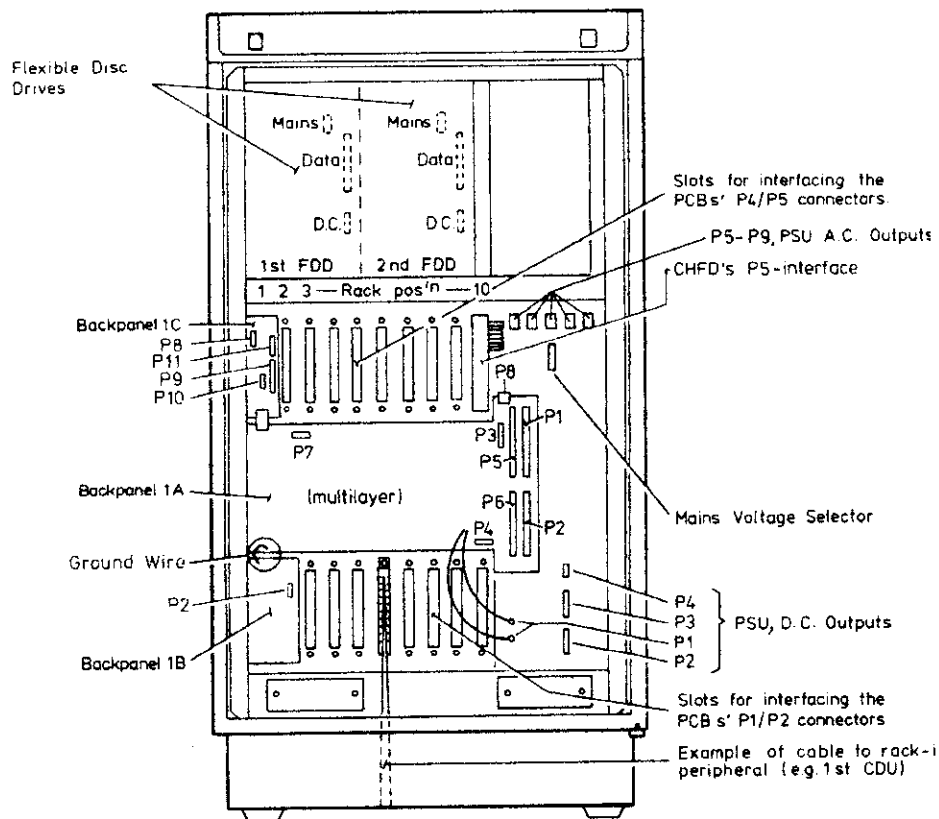
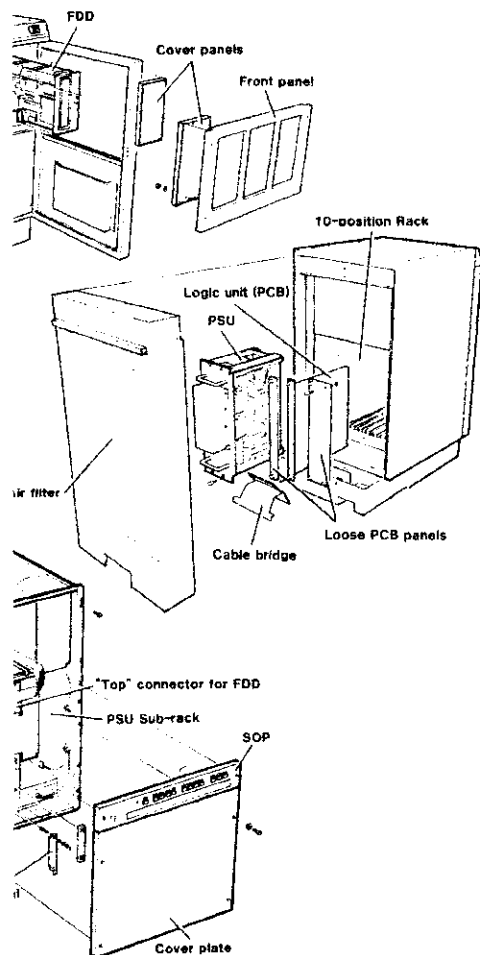
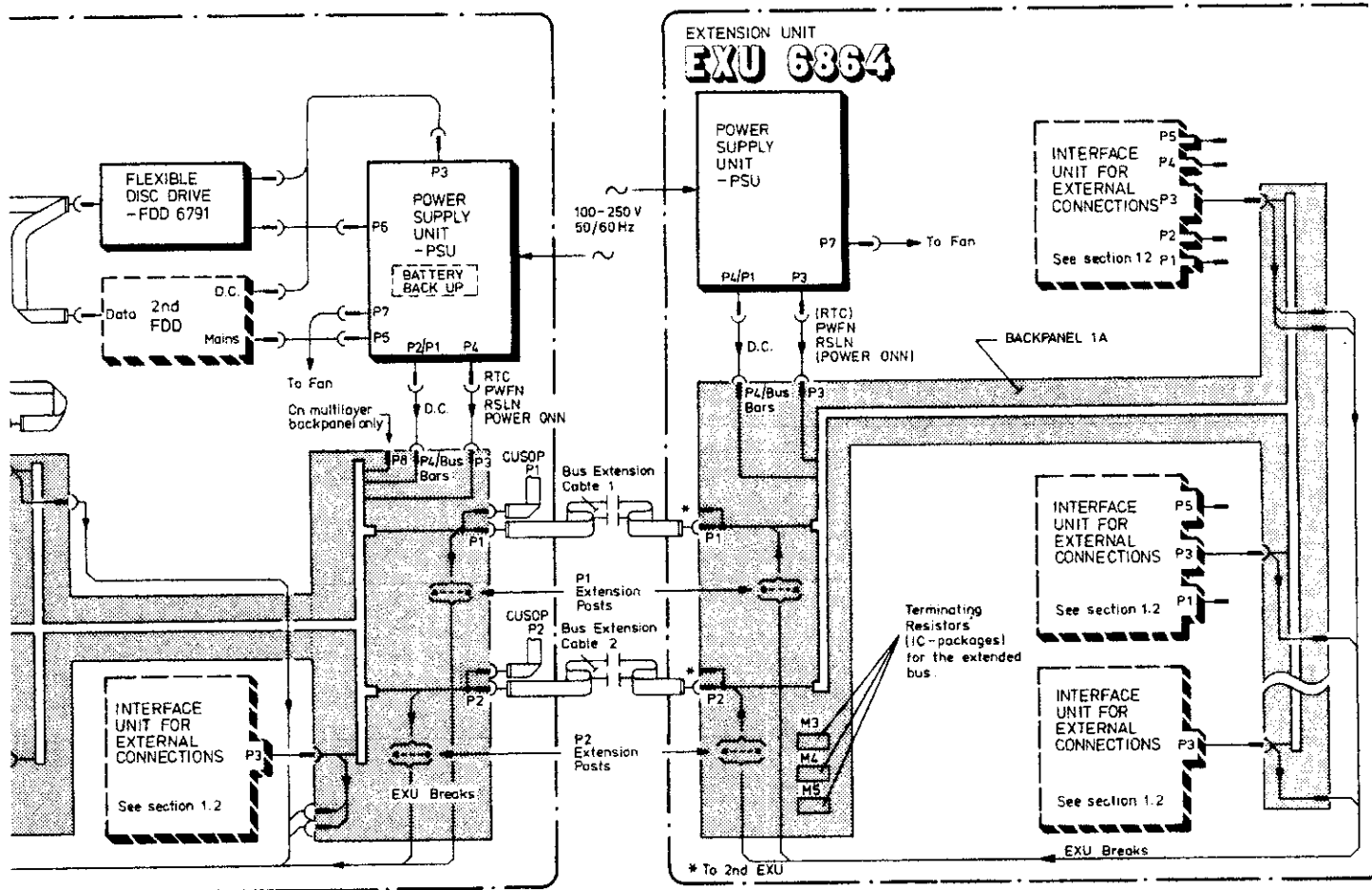


Figure 1.1-6 TC 6824/EXU 6864 - Basic Configuration







### 1.1.7 GENERAL PURPOSE (GP) BUS

All transfers of information between elements of the P852M/P856M or P857M system take place via the GP bus, and the lines of the bus comprise the input and output signal and address lines necessary for the data transfer requirements of the system. The GP bus can be extended outside the basic mounting box to further equipment shelves by using 125 Ohm, flexible, plug-in, transmission lines. The lines can be extended to convenient lengths between equipment shelves up to a total maximum length of 14.5 metres. Line termination facilities are provided in the basic mounting box and, if required, in the equipment shelves.

Two types of signal are used to bus: command signals and data signals. Command signals are those which will cause an immediate action according to their change of state: these signals have no unknown state but are always either logic "1" or "0". Data signals carry the actual information exchanged amongst the system elements: these signals are permitted to adopt indeterminate values except when the information is actually being used in the processing.

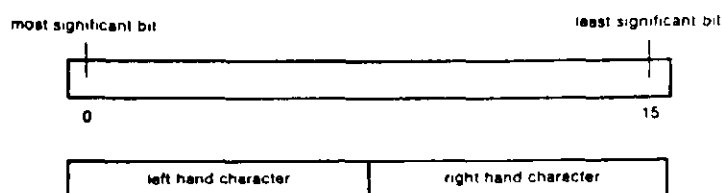
The signals carried by the GP bus lines are described below. When a mnemonic ends in "N" it means, in the case of a data signal, that the signal transmitted on the GP bus is the complementary value of the true signal. In the case of the control signal the "N" means that the signal performs its function on being set to "0" (active low). Most of the GP bus lines are used both inside and outside the basic mounting box. Where this does not apply it is indicated in the signal description given below.



**GP Bus Signals**  
**B10 00N to B10 15N**

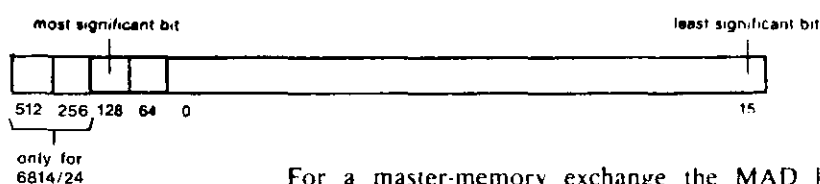
16 data lines which are used to carry data information between all system elements concerned with the transmission or reception of data signals.

The bit location is as follows:



**MAD128, 64 and 00 to 15**  
 (only MAD03, 04, 08-15  
 used externally also)

18 address lines which carry different information according to the type of exchange. The bit location is as follows:



For a master-memory exchange the MAD lines carry the memory address and MAD15 is used as a character indicator. When set to 1 it indicates the *right* (least significant) character and when set to 0 the left (most significant) character.

For a master-control unit exchange the lines MAD10-15 carry the address of the control unit and lines MAD 04, 08 and 09 the function to be performed. MAD03 indicates whether or not the exchange in progress is the last. The functions are as listed below:

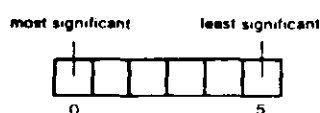
MAD04 = 0	exchange to control unit
MAD04 = 1	exchange to master
MAD08 = 0	data exchange (INR, OTR)
MAD08 = 1	command or status exchange
MAD09	special functions
MAD03 = 0	exchange not the last
MAD03 = 1	last exchange.

For a master-external register exchange the lines MAD08 to 15 carry the address of the external register. MAD04 is used to indicate whether it is a read or write operation as follows:

MAD04 = 0	write operation
MAD04 = 1	read operation.

**BIEC 0 to BIEC 5**

Six signal lines which represent in encoded form the interrupt raised (other than internal interrupts) having the highest priority. The format is as follows:



SCEIN		A signal <i>Scan External Interrupts</i> sent by the CPU to control units at the end of each instruction which places on the BIEC 0 to 5 lines the 6 bits representing the highest priority external interrupt detected.
ACN		A signal <i>function accepted</i> which is sent by a control unit to the CPU to indicate that the requested function is accepted by the control unit.
BUSRN	<div> <div></div> <div>Internal use only</div> </div>	A signal <i>bus request</i> which is sent to the bus controller in the CPU by a master which requires control of the bus to effect an exchange.
BSYN		A signal <i>bus busy</i> which is shared by all masters. It is set to "0" by the master which has been given control of the bus so that the exchange can commence without interruption.
MSN		A signal <i>master selected</i> which is transmitted to all other masters by the master which has become master of the bus to block all activity of the priority selection chain. The signal is released when the master is ready for the next priority transaction.
SPYC		(active low) A signal <i>scan priority chain</i> sent by the bus controller to all masters in response to a BUSRN signal. The signal enables the highest priority master which has transmitted BUSRN to block the priority chain at its level.
OKO (internal use only)		A signal generated by the bus controller after all masters have been alerted by SPYC. It is sent to the master having the highest priority (determined by hard wiring in the priority selection chain).
OKI (internal use only)		A master which receives signal OKO regards the signal as OKI. It then retransmits a further OKO to the next master in the priority chain. The first master to receive OKI set to '1' and to retransmit OKO reset to '0' is next master of the bus.
CHA (internal use only)		A signal <i>character</i> transmitted to the memory by the master which has control of the bus to indicate whether the exchange is to be by character or by word as follows: CHA = 1      character operation CHA = 0      word operation.
WRITE (internal use only)		A signal <i>write</i> transmitted to the memory by the master which has control of the bus to write information into memory or to read information from memory as follows: WRITE = 1    write into memory WRITE = 0    read from memory.
CLEARN		A signal <i>clear</i> transmitted by the CPU to all elements connected to the GP bus to cause a general reset to zero.



TMRN (internal use only)	A signal <i>master to memory</i> transmitted by a master to memory to validate the data on the BIQ and MAD lines during an exchange. The signal also controls the timing of the exchange.
TMPN	A signal <i>master to peripheral</i> transmitted by a master to a peripheral CU to validate the address of the peripheral CU and to initialize the exchange.
TMEN	A signal <i>master to external register</i> transmitted by a master to a unit containing the addressed register to validate the address and data of the register and to control the timing of the exchange.
TRMN	A signal <i>register or memory to master</i> transmitted by a unit controlling a register or by memory in reply to TMEN or TMRN to indicate that the unit transmitting the signal is in a condition to be read. The signal is also used to terminate the exchange.
TPMN	A signal <i>peripheral to master</i> transmitted by the peripheral control unit concerned in reply to TMPN. It is also used to validate the response of the control unit and to terminate the exchange.
RSLN	An Earth signal <i>reset line</i> transmitted by the CPU power supply (or external rack power supplies) and used to protect the peripherals during the switching on and switching off power sequence. The signal is also used to generate CLEARN when switching on.
PWFN	A signal <i>power fail</i> transmitted by the CPU power supply (or external rack power supplies) to warn the CPU that power failure has been detected. The signal is also used as a facility to restart the system at the point where it has been stopped.
4 spare lines	There are 4 spare lines provided on the GP bus extension cable outside the CPU cabinet.

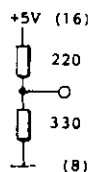
Backpanel 1A holds the signal-lines of the General Purpose Bus.

The following list shows the signal-names against the pin-numbers:

Note that the pins are numbered from bottom to top, the A-side at the right-hand side and the B-row at the left-hand side.

M1/15 --- MAD 128 - 3B43	● ● 3A43 - MAD 256/BR*
M1/14 --- MAD 64 - 3B42	● ● 3A42 - MAD 512/BR*
M1/13 --- MAD 00 - 3B41	● ● 3A41 - BR
M1/12 --- MAD 01 - 3B40	● ● 3A40 - GND
M1/11 --- MAD 02 - 3B39	● ● 3A39 - CLEARN
MAD 03 - 3B38	● ● 3A38 - BSYN ----- M1/10
MAD 04 - 3B37	● ● 3A37 - MSN ----- M1/9
M1/5 ---- MAD 05 - 3B36	● ● 3A36 - BUSRN ----- M1/7
M1/4 ---- MAD 06 - 3B35	● ● 3A35 - SPYC ----- M1/6
M1/3 ---- MAD 07 - 3B34	● ● 3A34 - ACN
MAD 08 - 3B33	● ● 3A33 - GND
MAD 09 - 3B32	● ● 3A32 - TPMN
MAD 10 - 3B31	● ● 3A31 - TMPN
MAD 11 - 3B30	● ● 3A30 - TMEN
MAD 12 - 3B29	● ● 3A29 - TMRN ----- M2/15
MAD 13 - 3B28	● ● 3A28 - TRMN
MAD 14 - 3B27	● ● 3A27 - CHA ----- M2/13
MAD 15 - 3B26	● ● 3A26 - WRITE ----- M2/12
+16 V - 3B25	● ● 3A25 - GND
GND - 3B24	● ● 3A24 - GND
+5 V - 3B23	● ● 3A23 - BR
0 V - 3B22	● ● 3A22 - 0 V
0 V - 3B21	● ● 3A21 - 0 V
+5 V - 3B20	● ● 3A20 - +5 V
+5 V - 3B19	● ● 3A19 - +5 V
-5 V - 3B18	● ● 3A18 - 0 V
RSLN - 3B17	● ● 3A17 - PWFN
OKI - 3B16	● ● 3A16 - OKO
BIO 15N - 3B15	● ● 3A15 - BIO 14N
BIO 13N - 3B14	● ● 3A14 - BIO 12N
BIO 11N - 3B13	● ● 3A13 - BIO 10N
BIO 09N - 3B12	● ● 3A12 - BIO 08N
BIO 07N - 3B11	● ● 3A11 - BIO 06N
BIO 05N - 3B10	● ● 3A10 - BIO 04N
BIO 03N - 3B09	● ● 3A09 - BIO 02N
BIO 01N - 3B08	● ● 3A08 - BIO 00N
0 V - 3B07	● ● 3A07 - 0 V
+16 V - 3B06	● ● 3A06 - +16 V
BIEC 5 - 3B05	● ● 3A05 - SCEIN
BIEC 3 - 3B04	● ● 3A04 - BIEC 4
BIEC 1 - 3B03	● ● 3A03 - BIEC 2
Chassis GND - 3B02	● ● 3A02 - BIEC 0
-18 V - 3B01	● ● 3A01 - +18 V

#### M1/M2 Ternets



\* Address lines in CPU and Memory positions,  
Break outputs in other positions.

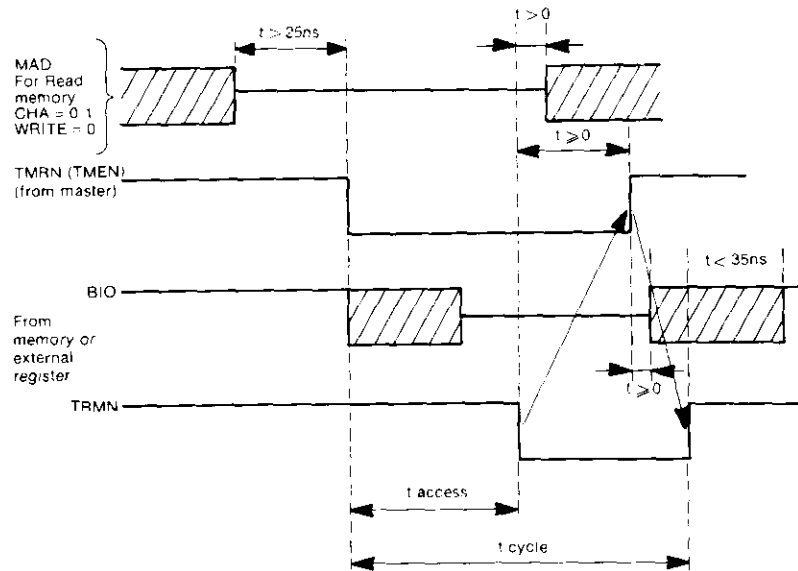


Figure 1.1-12 Timing Read Memory (or External Register)

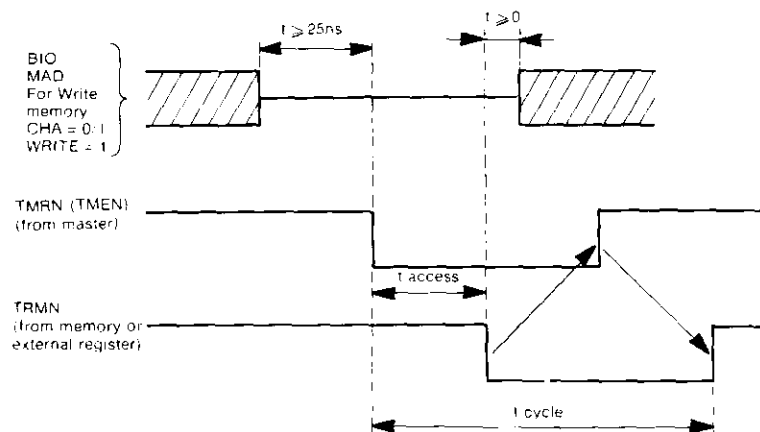
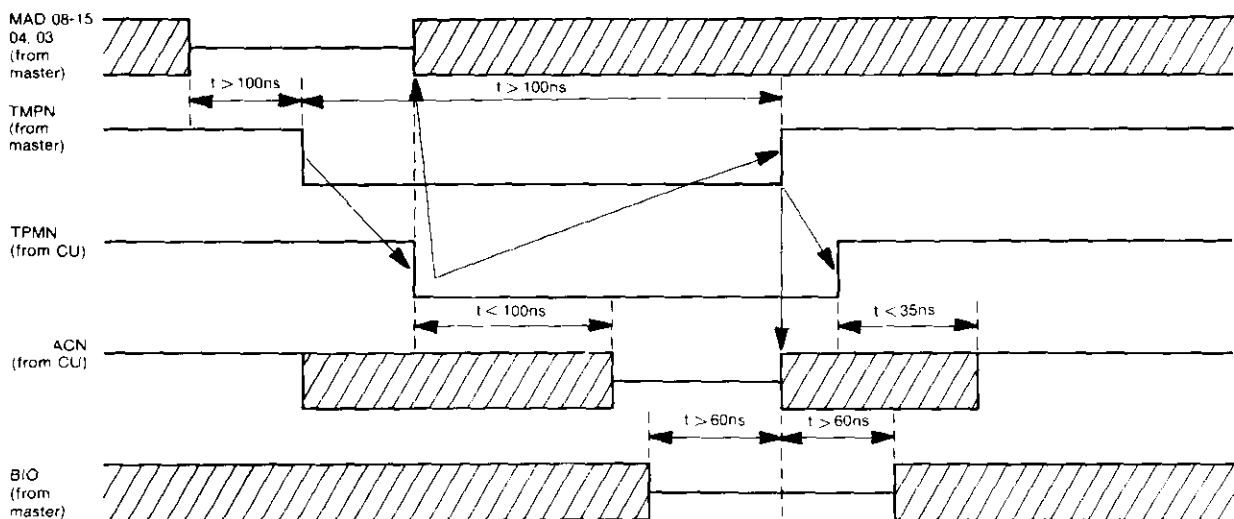


Figure 1.1-13 Timing Writing in Memory (or External Register)

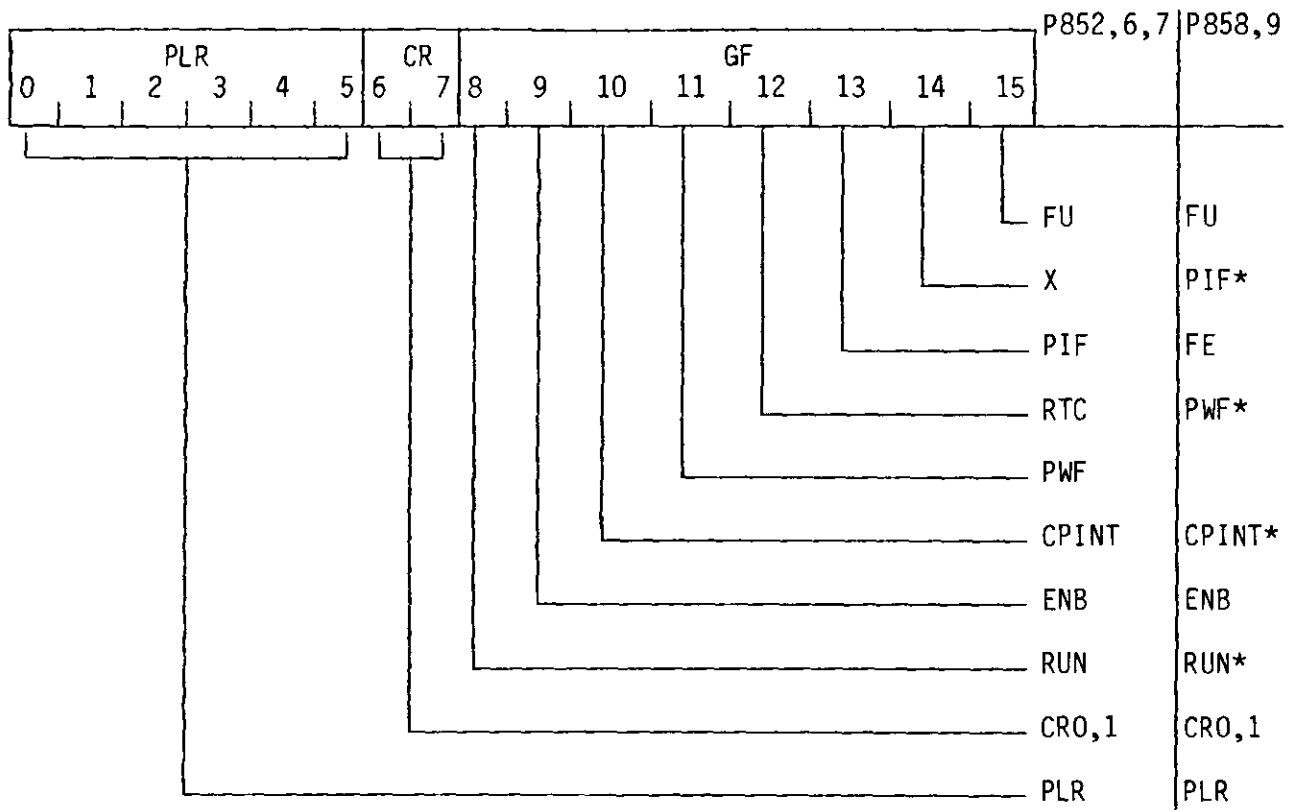


Note: CU which recognises its address specifies accept or not accept function using ACN. If function accepted CU must stabilize data presented at least 60 ns before TMPN goes high again. Data must remain present at least 60 ns after TPMN goes high.

Figure 1.1-14 Timing for an OTR Exchange



### 1.1.8 PROGRAM STATUS WORD (PSW)



FE : Extended System Mode  
 FU : User Mode  
 RTC : Real Time Clock  
 PWF : Power Failure Interrupt  
 CPint : Control Panel Interrupt  
 ENB : Interrupt ENable  
 RUN : CPU in RUN Mode  
 CR : Condition Register  
 PLR : Program Level Register  
 PIF : Program Interrupt, Stack Overflow\*\*

\* These bits are not displayable (blanked in microprogram).

CRO CR1	ARITHMETIC	COMPARE	I/O
00	Zero	Equal	Accepted
01	Positive	Greater	Not Accepted
10	Negative	Less	--
11	Overflow	--	Device Address Unknown

\*\* Stackoverflow if (A15) smaller than /100.

## 1.1.9 INTERRUPT SYSTEM

### Interrupt levels internal

HEX	LEVEL DEC	Interr. control Address HEX	SOURCE
0	0	0	PF/AR
1	1	2	LKM/Stackoverflow;(A15),Less than /100
2	2	4	RTC
3	3	6	Not Used
4	4	8	Not Used
5	5	A	Not Used
6	6	C	Control Panel
7	7	E	Console Typewriter
.	.	.	.
.	.	.	.
1F	31	2E	Page Fault MMU for 6813 (depends on strap setting MMU)
.	.	.	.
.	.	.	EXTERNAL LEVELS SEE CHAPTER 2.5
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
.	.	7A*	TC6814/24 Page Fault Trap
.	.	7C*	TC6814/24 D Type Trap
3E	63	7E*	Trap control address for invalid or priveleged instructions

\* PLR not changed

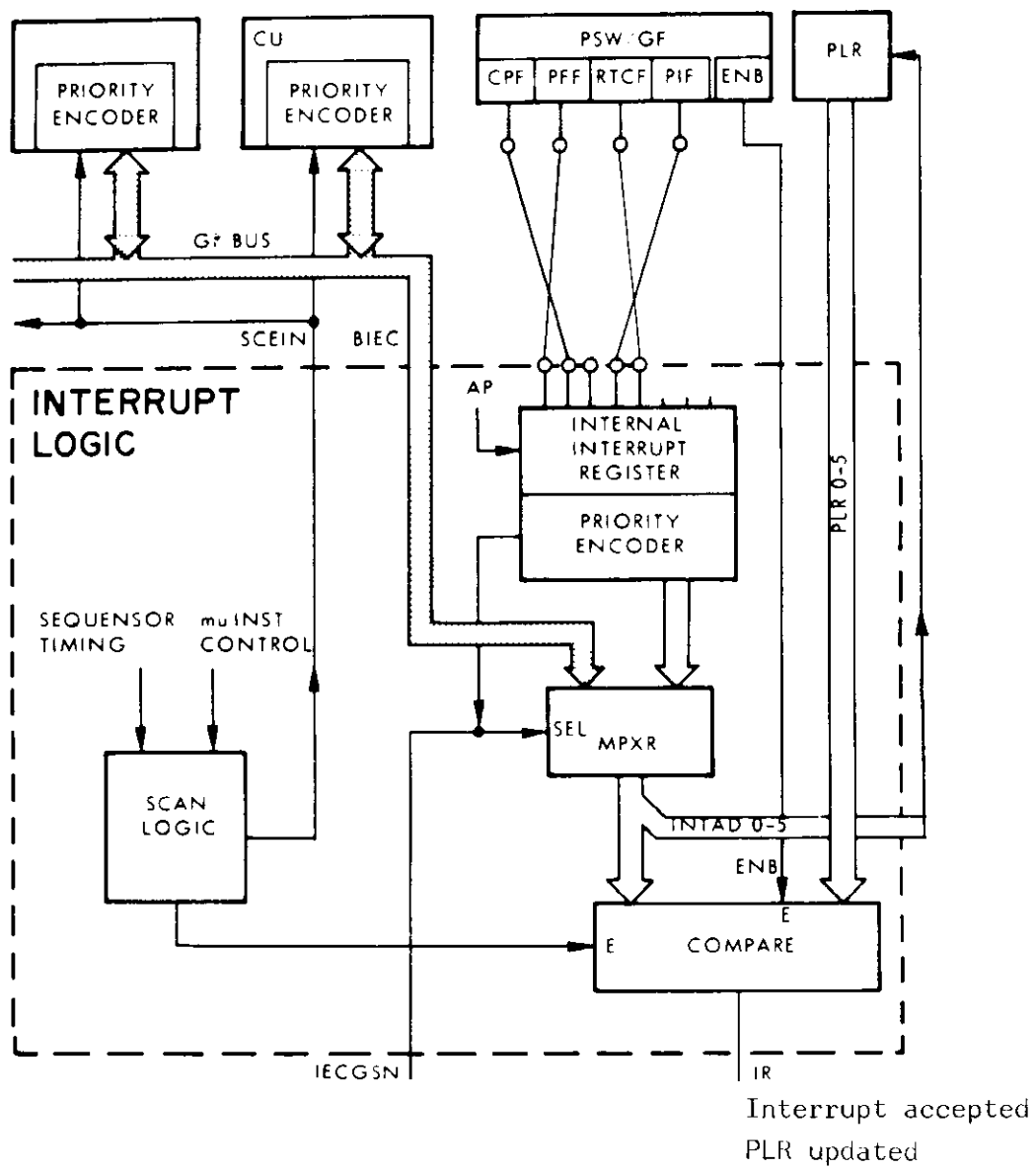
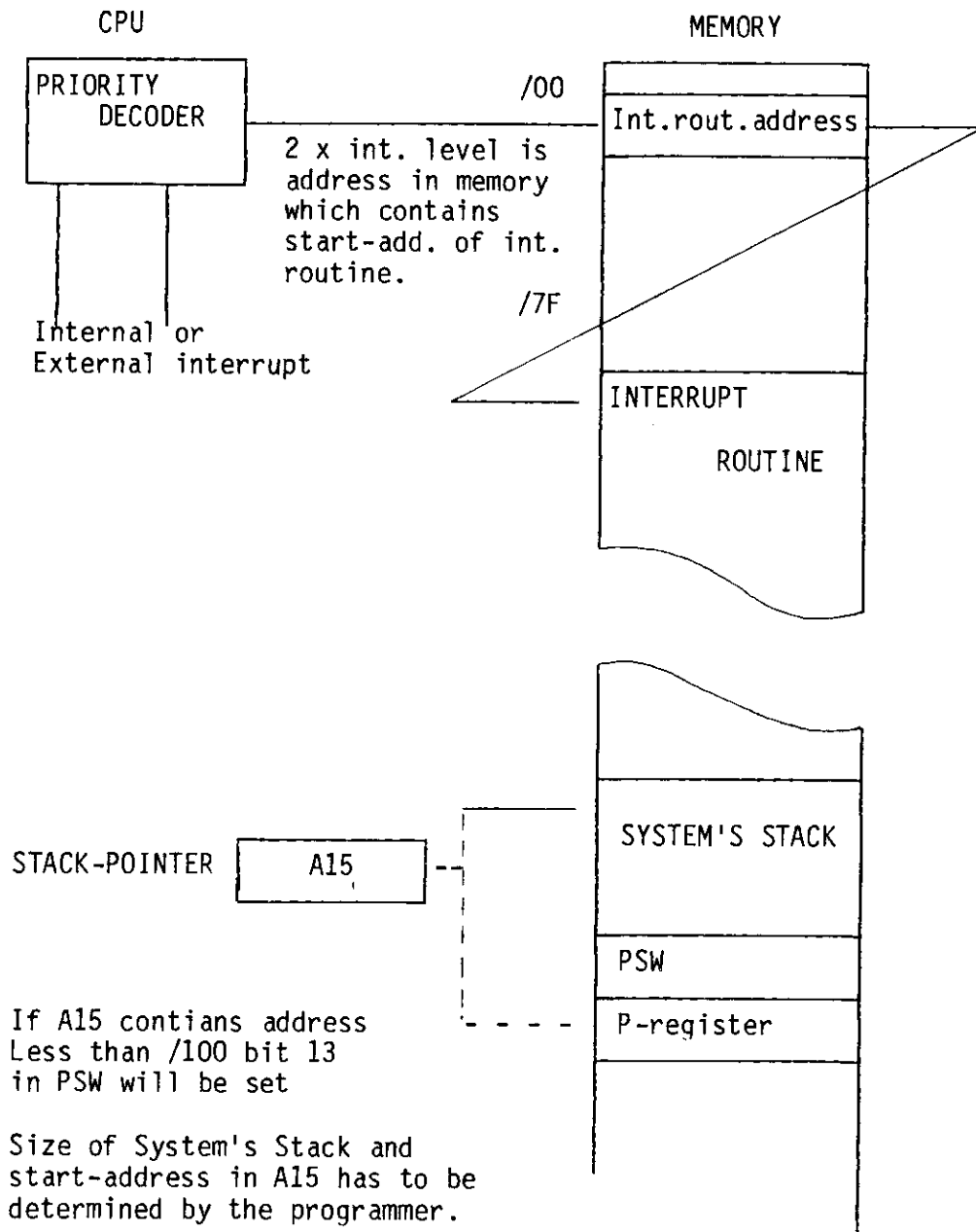


Figure 1.1-17 Interrupt System





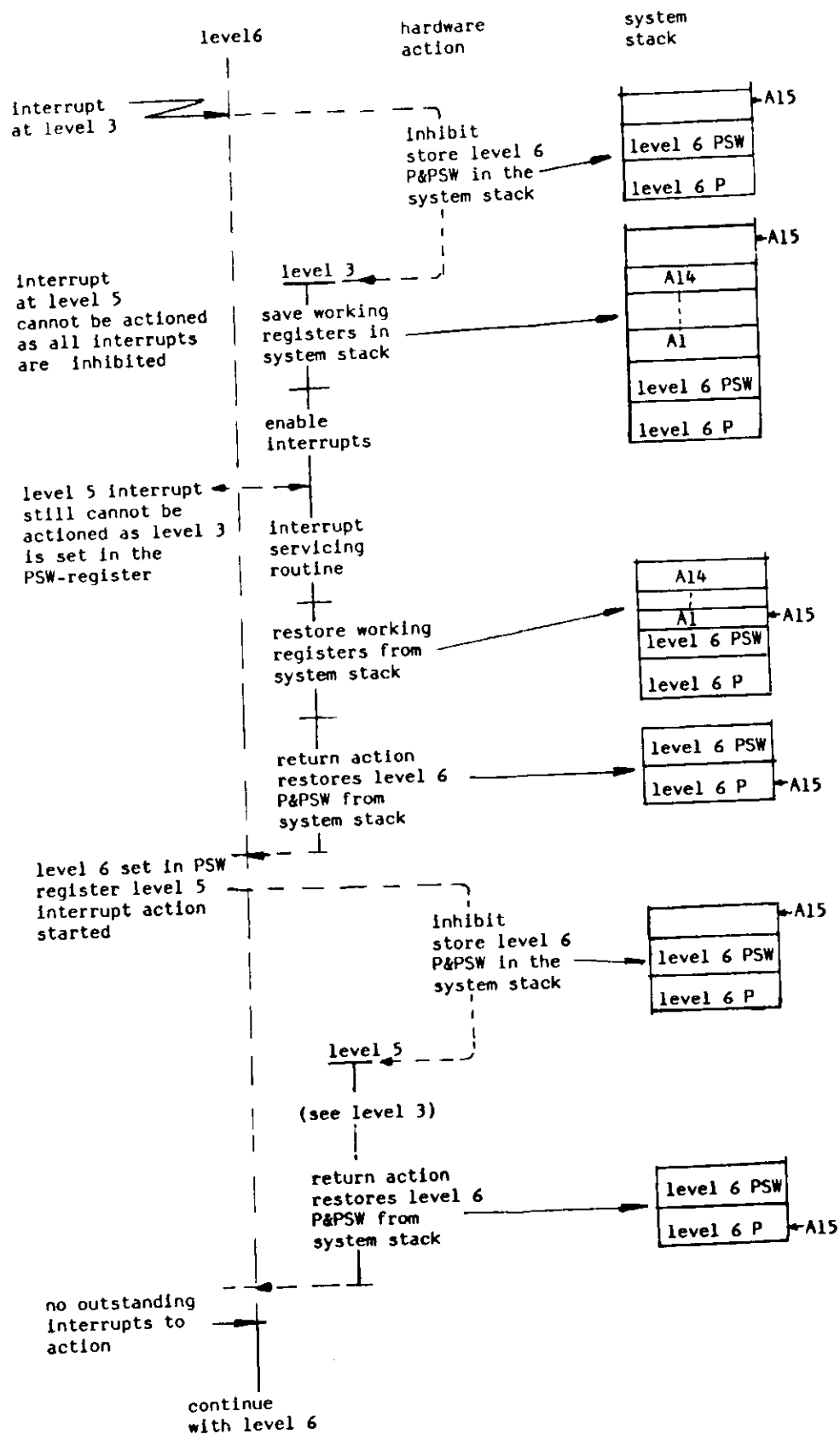


Figure 1.1-18 Diagram of Interrupt Sequence

### 1.1.10 I/O CHANNEL

Control Unit Modes:

Example:

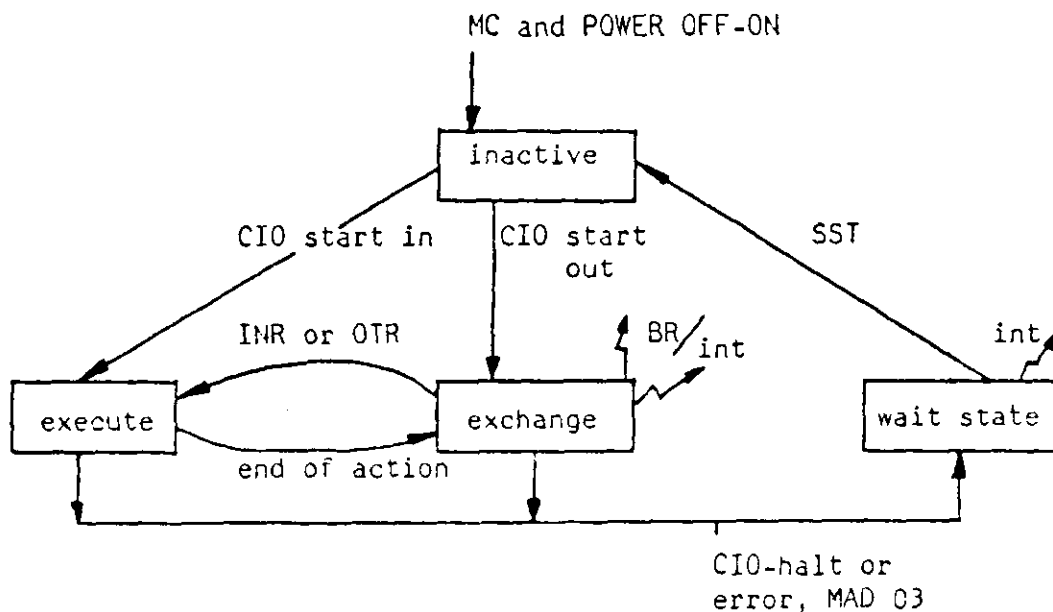
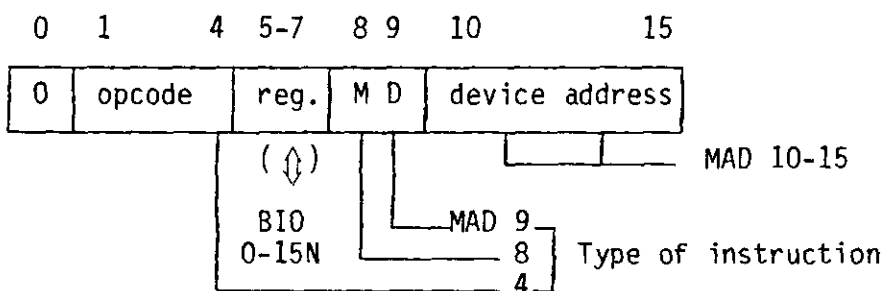


Figure 1.1-19 Control Unit Modes

### I/O Instructions Format



Instruction Bits	4	8	9		
MAD Lines	03	04	08	09	Accepted in mode
CIO Start	0	0	1	1	Inactive
CIO Stop	0	0	1	0	Always
INR (Input Transfer)	0	1	0	0	Exchange
OTR (Output Transfer)	0	0	0	0	Exchange
TST (Test Status)	0	1	1	0	Always
SST (Send Status)	0	1	1	1	Wait state
INR (last) IOP	1	1	0	0	Exchange
OTR (last) IOP	1	0	0	0	Exchange

# CONDITION REGISTER (DISPLAYS TPMN AND ACN - LINES)

0 0 = accepted  
 0 1 = not accepted  
 1 1 = device address not recognized

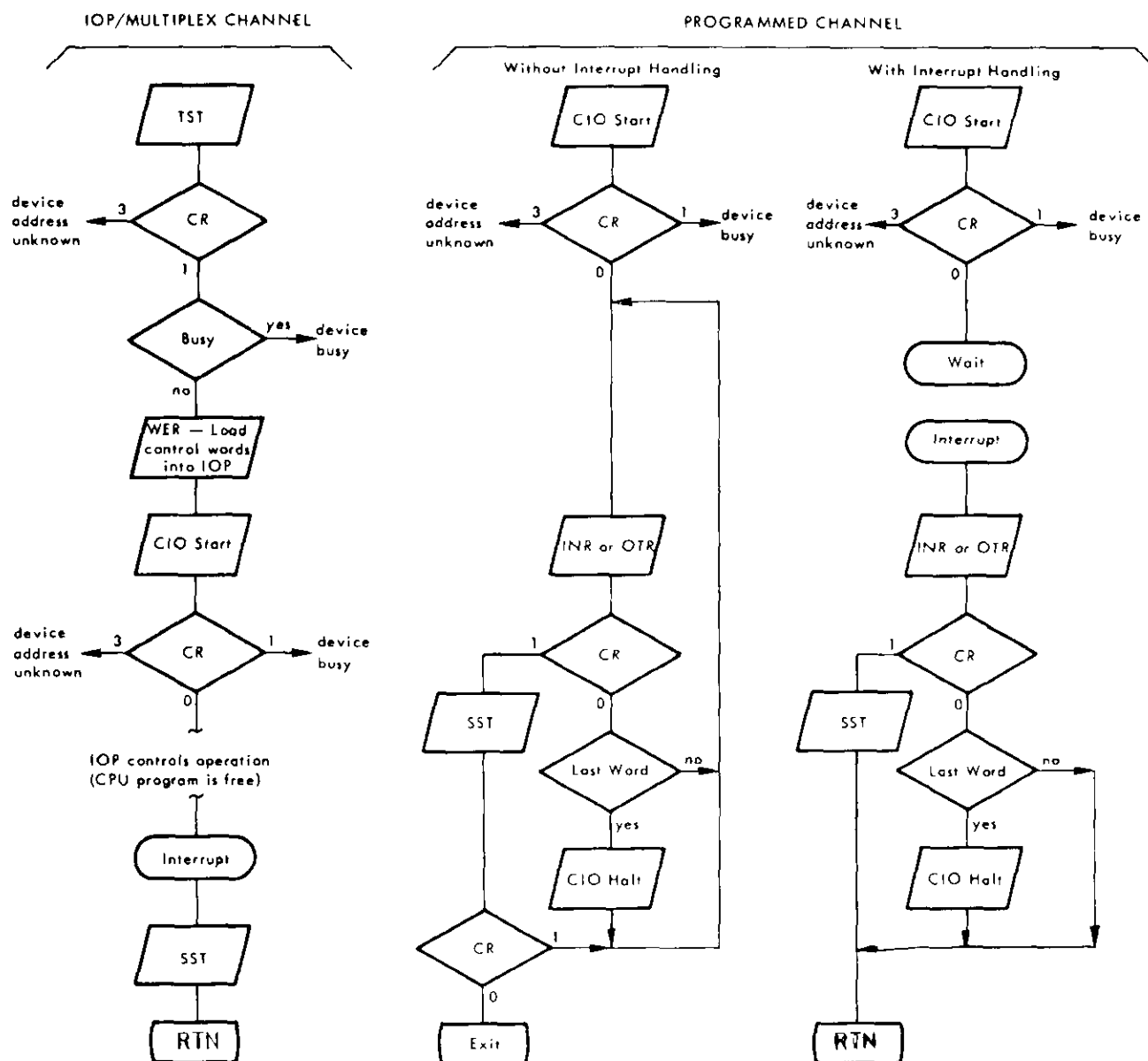


Figure 1.1-20 General Programming Sequence

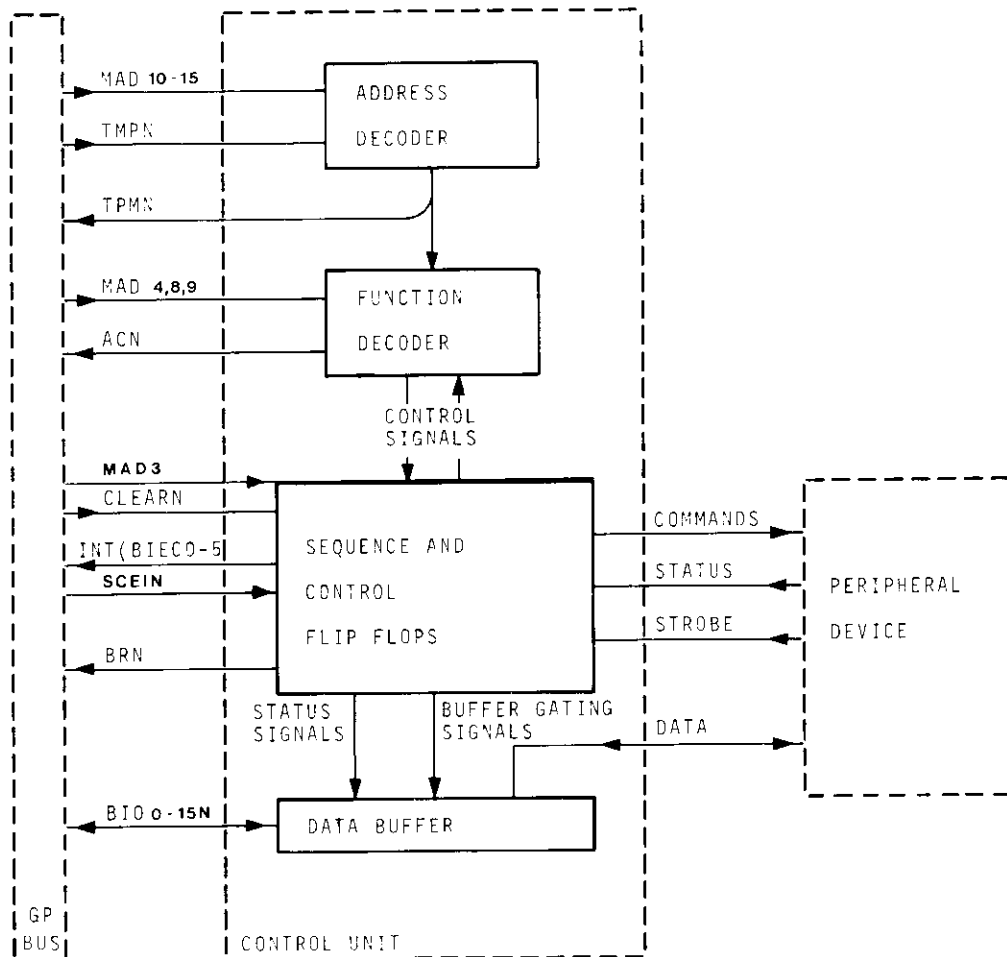
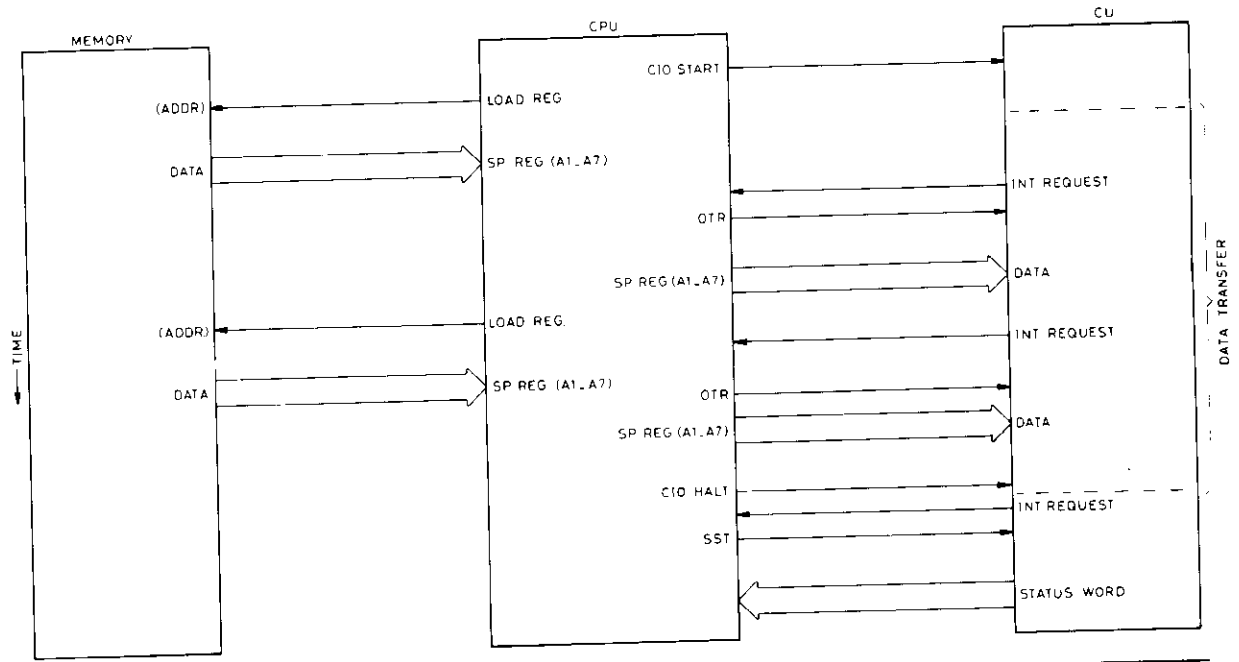
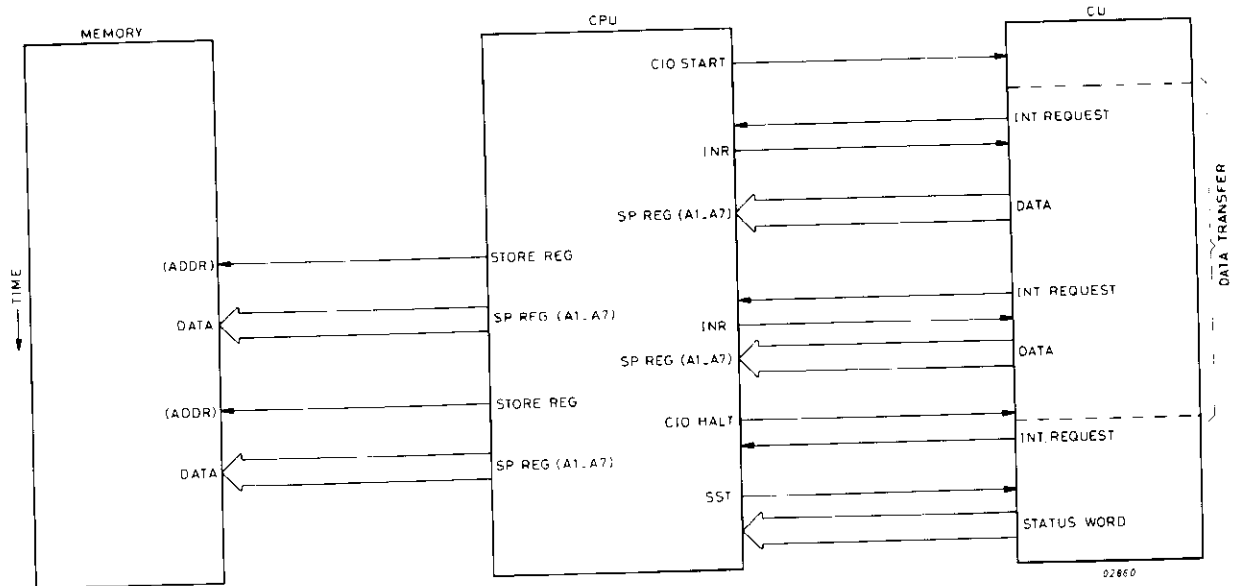


Figure 1.1-21 Block Diagram of Typical Control Unit

# OUTPUT TRANSFER

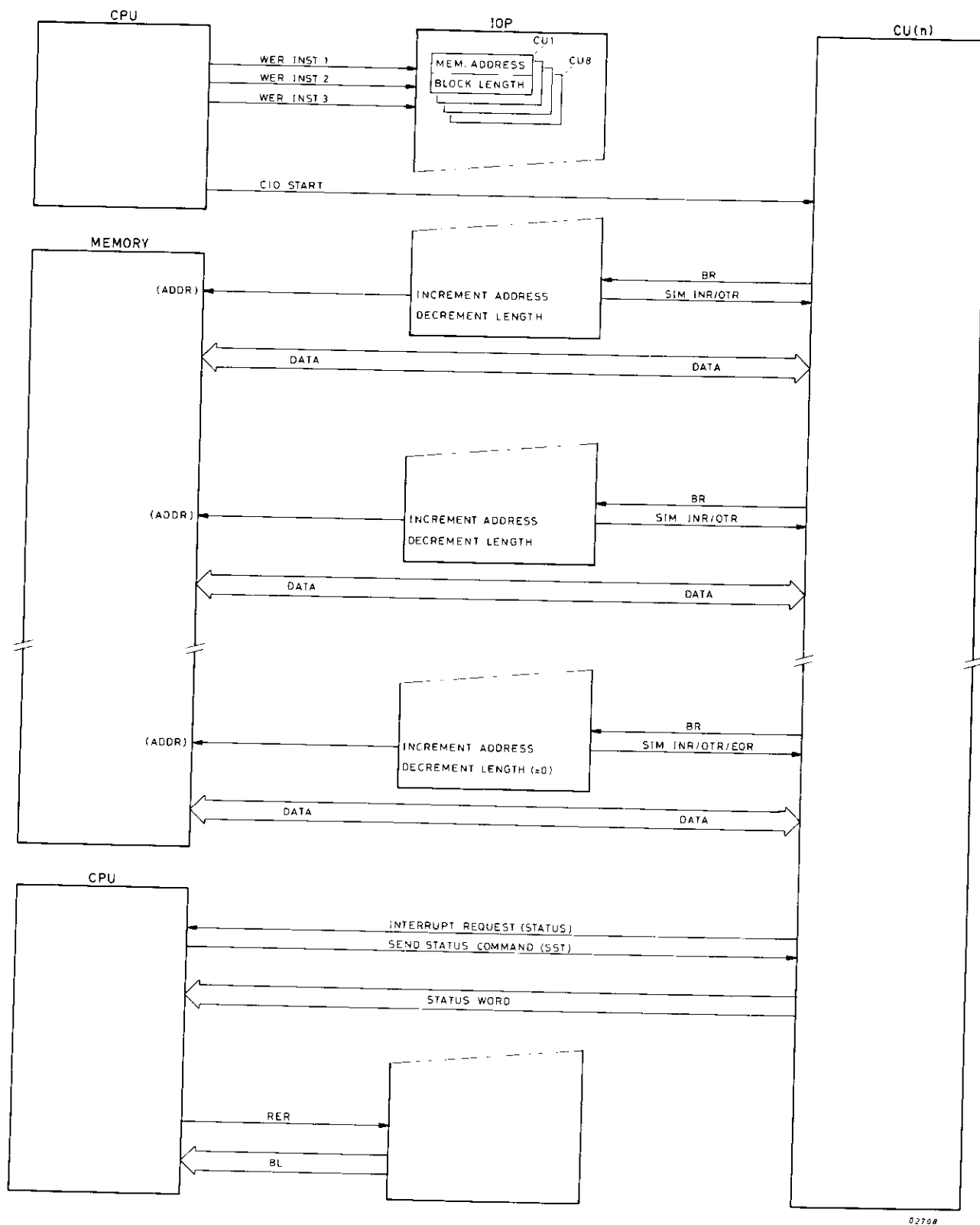


# INPUT TRANSFER



## PROGRAMMED CHANNEL TRANSFERS

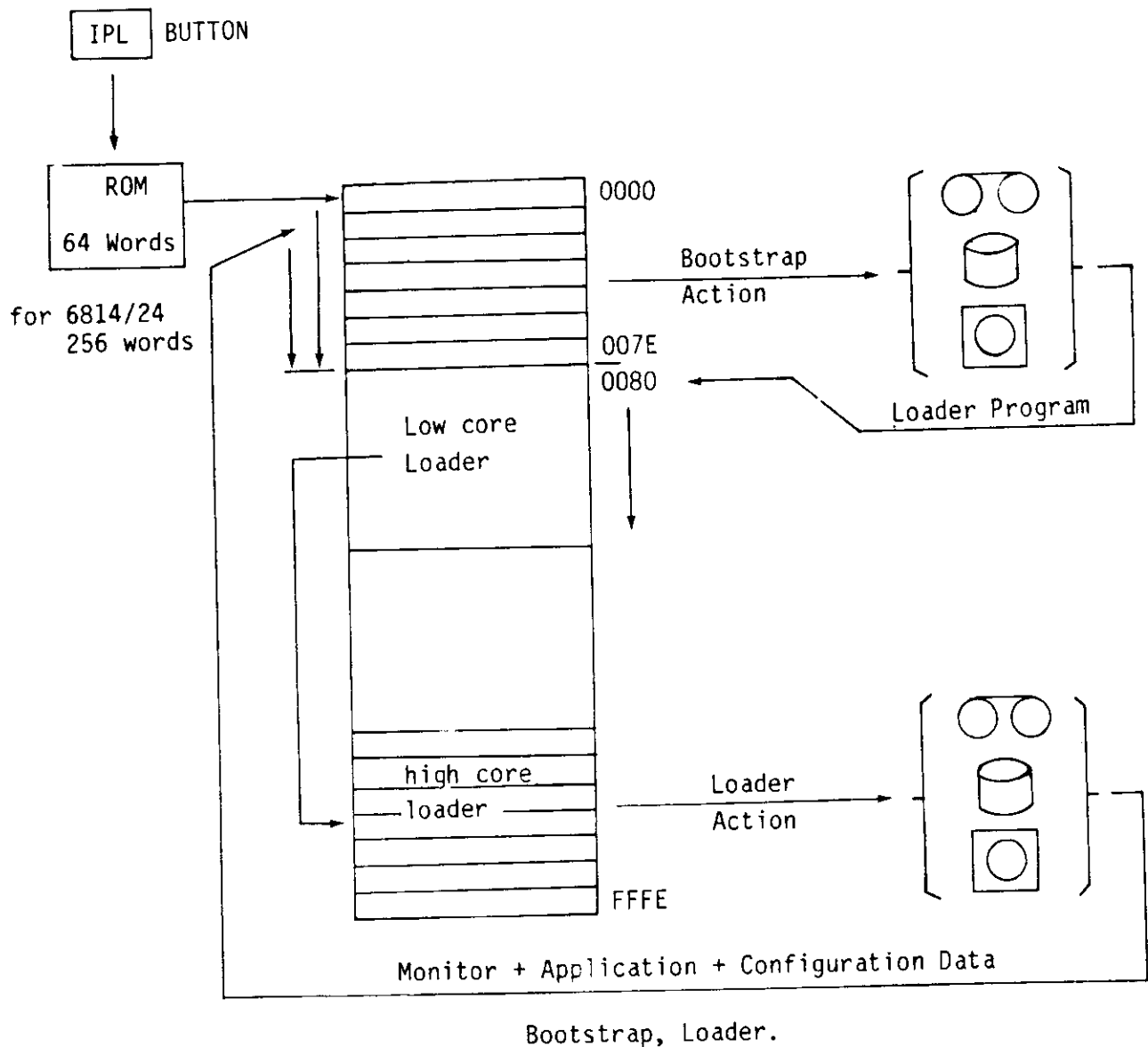
"Only 2 WER instructions for PTS6811/12/13"



02798

Note-- This diagram shows the sequence for transferring a block of data between memory and single CU, (n). The IOP can multiplex up to eight CUs; the operation shown is thus duplicated for each CU.

### 1.1.11 IPL PROCEDURE



DATE 82-05-05 IDENT LOWCOR

```

0000          IDENT      LOWCOR
0001          *DATE: 820505 FOR PTS
0002          *          EXAMPLE LOW CORE LOADER CASSETTE
0003          AORG      /80
0004
0005 0080 FFFE      FLAG      DATA      /FFFE
0006 0082 0000      DATA      0
0007 0084 90A1 0080  LOWSTA    IM          FLAG      INCREMENT FLAG
0008 0088 501A      RF(0)      SECOND      IS IT FIRST OR SECOND TIME
0009          *          FIND OUT MEMORY SIZE
0010 008A 8720 5555  FIRST     LDKL      A7:/5555
0011 008E 81A0 FF78      LDKL      A9:/FF78      ADDR HIGH CORE LOADER IF 32 KW MEM
0012 0092 8727      MSIZE     STR        A7,A9      STORE (A7)
0013 0094 EF26      CWR*      A7,A9      CHECK IF MEM CONT IS (A7)
0014 0096 5006      RF(0)      UPDREG      YES UPDATE REG FOR HIGH CORE LOAD
0015 0098 99A0 1000  NO        SUKL      A9:/1000    DECREMENT ADDR HIGH CORE
0016 009C 5F0C      RB        MSIZE
0017          *          UPDATE REGISTERS TO LOAD HIGH CORE LOADER
0018 009E 0588      UPDREG    LDK        A5:/88      NUMBER OF CHARACTERS HIGH CORE LOADER
0019 00A0 8604      LDR        A6,A9      FIRST ADDR HIGH CORE
0020 00A2 0F42      AB        /42      BRANCH TO BOOTSTRAP FOR HIGH CORE LOAD
0021          *          START HIGHCORE LOADER
0022 00A4 8120 0400  SECOND    LDKL      A1:/0400
0023 00A8 412E      QTR        A1,0:/2E      LIGHT LOAD LAMP ON SOP
0024 00AA 8386      LDR        A11,A9      SAVE HIGH CORE START ADDR
0025 00AC 9986      SUR        A9,A9      CLEAR A9
0026 00AE 9C92      SUR        A12,A12     CLEAR A12
0027 00B0 86A0 FFFB      LDKL      A14:/FFFB
0028 00B4 8F0E      ABR        A11      BRANCH TO HIGH CORE LOADER
0029          END          FLAG

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0000          IDENT      HIGHCOR
0001          *DATE: 820505 FOR PTS
0002          AORG      /FF7B
0003          *          EXAMPLE HIGH CORE LOADER FOR CASSETTE
0004
0005 FF7B 8500      HIGHST  LDR      A5,0          SAVE HIGH CORE START ADDR
0006 FF7A 1D02      SUK      A5,2
0007 FF7C 02C0      LDK      A2,/C0
0008 FF7E 3B64      SRL      A3,4
0009 FF80 2301      ANK      A3,/01
0010 FF82 920C      ADR      A2,A3
0011 FF84 8306      LDR      A3,A9
0012 FF86 0700      LDK      A7,0
0013 FF88 0600      A3IA13  LDK      A6,0
0014 FF8A 840C      LDR      A4,A3
0015 FF8C 010A      READH   LDK      A1,/0A      READ BLOCK
0016 FF8E 41CE      CIO      A1,1,/0E
0017 FF90 490E      INRH    INR      A1,0,/0E
0018 FF92 540B      RF(4)   SSTH
0019 FF94 EC14      CWR      A4,A5      IS THERE MEMORY OVERFLOW
0020 FF96 505E      RF(0)   MEMOFL
0021 FF98 E131      STPROG  SCR      A1,A4
0022 FF9A 1401      ADK      A4,1      INCREMENT MEM ADDR
0023 FF9C 49CE      SSTH    SST      A1,/0E      STATUS?
0024 FF9E 5C10      RB(4)   INRH
0025 FFA0 A120 FCFE  CHSTAT  ANKL    A1,/FCFF      CHECK ON STATUS ERROR
0026 FFA4 543A      RF(4)   STATER
0027 FFA6 1C10      SUK      A4,/10
0028 FFA8 B590      LDR      A13,A4
0029 FFAA 1C02      SUK      A4,2
0030 FFAC 1402      ADK      A4,2
0031 FFAE 0610      A6ZERO  LDK      A6,/10
0032 FFB0 871C      LDR      A7,A7
0033 FFB2 501E      RF(0)   A7ZERO
0034 FFB4 B130      LDR*    A1,A4
0035 FFB6 5606      CHA1    RF(6)   A1NEG
0036 FFB8 B2AC      LDR*    A10,A3
0037 FFB9 92B6      ADR      A10,A9
0038 FFB0 5702      RF      COUNT
0039 FFB8 B2AC      A1NEG  LDR*    A10,A3
0040 FFC0 B2CD FFFB  CONT    ST      A10,/FFFB,A3
0041 FFC4 1302      ADK      A3,2
0042 FFC6 EB16      CWR      A3,A13
0043 FFC8 5B42      RB(0)   A3IA13
0044 FFCA 1E01      SUK      A6,1
0045 FFCC 5B20      RB(0)   A6ZERO
0046 FFCE 3941      SLL      A1,1
0047 FFD0 5F1C      RB      CHA1
0048 FFD2 872C      A7ZERO  LDR*    A7,A3
0049 FFD4 9706      ADR      A7,A9
0050 FFD6 130B      ADK      A3,8
0051 FFD8 1E04      SUK      A6,4
0052 FFDA B130      LDR*    A1,A4
0053 FFDC 3944      SLL      A1,4
0054 FFDE 5F2A      RB      CHA1
0055 FFE0 39C3      STATER  SLC      A1,3
0056 FFE2 5610      RF(6)   ERROR
0057 FFE4 462E      QTR      A6,0,/2E
0058 FFE6 1B0B      SUK      A3,8
0059 FFE8 B18C      LDR      A9,A3
0060 FFEA B59C      LDR      A13,A7
0061 FFEC 8492      LDR      A12,A12
0062 FFE4 5402      RF(4)   BRA12
0063 FFF0 8F16      ABR      A13
0064 FFF2 8F12      BRA12  ABR      A12
0065 FFF4 1601      ERROR  ADK      A6,1
0066 FFF6 1601      MEMOFL ADK      A6,1
0067 FFF8 E61B      ECR      A6,A6
0068 FFFA 462E      QTR      A6,0,/2E      ERROR DISPLAY ON60P
0069 FFFC 207F      HLT
0070 FFFE 5F8B      RB      HIGHST
*S          0000 5F8B
*****
0071          END      HIGHST

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# 1.1.12 CONTENTS IPL PROM 5131 110 01142

DATE	82-05-05	IDENT	B1142	820505
0000		IDENT	B1142	820505
0001		FOR IPL FROM CASSETTE, 2.5M AND 5M DISC AND MAGNETIC TAPE		
0002		CONTENTS OF A3 FOR SOP SWITCHES:		
0003	*SW1	/FE00	DCR DRIVE 0	
0004	*SW2	/FD00	DCR DRIVE 1	
0005	*SW3	/FCB0	CARTRIDGE DISC DRIVE 0	
0006	*SW4	/FC40	FIXED DISC DRIVE 0	
0007	*SW5	/FC20	MAGNETIC TAPE DRIVE 0	
0008	*SW6	/FC10	NOT USED	
0009	*SW7	/FC08	NOT USED	
0010	*SW8	/FC04	NOT USED	
0011	*SW9	/FC02	NOT USED	
0012	*SW10	/FC01	NOT USED	
0013				
0014				
0015	0000 41EE	BOOT	CIO A1,1,/2E	START SOP
0016	0002 4B2E		INR A3,0,/2E	READ SOP SWITCH
0017	0004 5C04		RB(NA) *-2	
0018	0006 41AE		CIO A1,0,/2E	STOP SOP
0019	0008 3BA4		SRN A3,A1	WHAT SWITCH
0020	000A 1905		SUK A1,5	IS THE SWITCH LEGAL?
0021	000C 5A0E		RB(N) BOOT	NO READ NEXT SWITCH
0022	000E E444 0022 R		LC A4,DEVADR,A1	LOAD DEVICE ADDRESS
0023	0012 243F		ANK A4,/3F	
0024	0014 027B		LDK A2,SIO1-BOOT	ADDRESS OF CIO START
0025	0016 AC29		ORRS A4,A2	CHANGE DEVICE ADDRESS IN CIO
0026	0018 027A		LDK A2,SSTI-BOOT	ADDRESS OF SST
0027	001A AC29		ORRS A4,A2	CHANGE DEVICE ADDR IN SST
0028	001C 87A0 63CB		LDKL A15,/63CB	INIT A15 FOR DISC IPL
0029	0020 AF90		ORR A15,A4	MODIFY BY DA
0030	0022 0420	DEVADR	DATA /0420	USED FOR DEV ADDR EXECUTED AS LDK A2,/20
0031	0024 0806		DATA /0806	EXECUTED AS AB(0) /06 IS NOP
0032	0026 0680		LDK A6,/80	BASE ADDRESS LOW CORE LOADER
0033	0028 027B		LDK A2,EXCOM-BOOT	START ADDRESS COMMAND ROUTINE
0034	002A 1901		SUK A1,1	IS IT MAGNETIC TAPE
0035	002C 5226		RF(N) MTAP	
0036	002E 1902		SUK A1,2	IS IT DISC
0037	0030 5234		RF(N) DISC	
0038	0032 3101	CASS	XRK A1,1	SELECT DRIVE
0039	0034 F409		CFR A4,A2	
0040	0036 0102		LDK A1,2	LOCK SELECTED DRIVE
0041	0038 F409		CFR A4,A2	
0042	003A 0108		LDK A1,8	SEARCH BEGIN OF TAPE
0043	003C F409		CFR A4,A2	
0044	003E 010C		LDK A1,/C	SEARCH TAPE MARK
0045	0040 F409		CFR A4,A2	
0046	0042 010A	CASS10	LDK A1,/A	READ 1 BLOCK
0047	0044 41CE		CIO A1,1,/0E	START CHCR
0048	0046 490E	CASS20	INR A1,0,/0E	READ CHARACTER
0049	0048 5404		RF(NA) CASS30	IF NOT ACCEPTED CHECK STATUS
0050	004A E139		SCR A1,A6	STORE CHARACTER IN MEMORY
0051	004C 1601		ADK A6,1	INCREMENT MEM ADDRESS
0052	004E 49CE	CASS30	SST A1,/0E	GET STATUS
0053	0050 5C0C		RB(NA) CASS20	IF NOT ACCEPTED READ NEXT CHARACTER
0054	0052 0FB4		AB /B4	START LOW CORE LOADER
0055	0054 0151	MTAP	LDK A1,/51	ON LINE
0056	0056 F409		CFR A4,A2	
0057	0058 0124		LDK A1,/24	SEARCH FILE MARK
0058	005A F409		CFR A4,A2	
0059	005C 05FF		LDK A5,/FF	FIRST CONTROL WORD IOP
0060	005E 7518		WER A5,/1B	WRITE FIRST CONTROL WORD
0061	0060 7619		WER A6,/19	SECOND CONTROL WORD
0062	0062 0102		LDK A1,2	READ 1 BLOCK
0063	0064 570E		RF EXIT	
0064	0066 0103	DISC	LDK A1,3	SEEK TO ZERO
0065	0068 F409		CFR A4,A2	
0066	006A B120 80CD		LDKL A1,/80CD	FIRST CONTROL WORD
0067	006E 7110		WER A1,/10	WRITE FIRST CONTROL WORD TO IOP
0068	0070 7611		WER A6,/11	AND THE SECOND
0069	0072 010C		LDK A1,/C	READ SECTOR NUMBER 3
0070	0074 F409	EXIT	CFR A4,A2	
0071	0076 0FB4		AB /B4	START LOW CORE LOADER
0072	0078 0078	EXCOM	EGU *	
0073	007B 41CB		CIO A1,1,8	START CONTROLLER
0074	007A 4BCB	SSTI	SST A3,8	GET STATUS
0075	007C 5C04		RB(NA) *-2	
0076	007E F030		RTN A4	
0077				
0078				
0079				
0080		END	BOOT	

# 1.1.13 CONTENTS IPL PROM 4011P

DATE	B2-05-05	IDENT	B4011P
0000		IDENT	B4011P
0001		*DATA: 820505 FOR PTS	
0002		* FOR IPL FROM CASSETTE, FLEX DISC AND 2.5 AND 5M DISC	
0003		* CONTENTS OF A5 FOR SOP SWITCHES	
0004		*SW1 /FE00 DCR DRIVE 0	
0005		*SW2 /FD00 DCR DRIVE 1	
0006		*SW3 /FCB0 CARTRIDGE DISC DRIVE 0	
0007		*SW4 /FC40 FIXED DISC DRIVE 0	
0008		*SW5 /FC20 FLD DRIVE 0 (MUX)	
0009		*SW6 /FC10 FLD DRIVE 1 (MUX)	
0010		*SW7 /FC08 FLD DRIVE 0 (PC)	
0011		*SW8 /FC04 FLD DRIVE 1 (PC)	
0012		*SW9 /FC02 NOT USED	
0013		*SW10 /FC01 NOT USED	
0014			
0015			
0016	0000 44EE	START CIO	A4,1,/2E START SOP
0017	0002 4D2E	INR	A5,0,/2E READ SOP SWITCH
0018	0004 5C04	RB(4)	*-2
0019	0006 44AE	CIO	A4,0,/2E STOP SOP
0020	0008 3DB0	SRN	A5,A4 WHAT SWITCH IS DEPRESSED
0021	000A E350 001B	LC	A3,/1B,A4
0022	000E 233F	ANK	A3,/3F
0023	0010 0254	LDK	A2,/54 ADDR CIO INSTR
0024	0012 AB29	ORRS	A3,A2 MODIFY CIO START
0025	0014 0660	LDK	A6,/60 ADDR SST INSTR
0026	0016 AB39	ORRS	A3,A6 MODIFY SST
0027	0018 8520 80CD	LDKL	A5,/80CD FIRST CONTR. WORD IOP FOR DISC
0028	001C E719	DATA	/E719 EXECUTED AS ECR A7,A6
0029	001E 0911	AB(1)	/11
0030	0020 0120	LDK	A1,/20 STACKPOINTER
0031	0022 0806	AB(0)	/6
0032	0024 0680	LDK	A4,/80 FIRST ADDRESS OF LOW CORE LOADER
0033	0026 1C04	SUK	A4,4 IPL FROM WHAT DEVICE
0034	0028 5240	RF(2)	FLDPC
0035	002A 1C02	SUK	A4,2
0036	002C 5248	RF(2)	FLDMUX
0037	002E 1C02	SUK	A4,2
0038	0030 5214	RF(2)	DISC
0039	0032 3401	XRK	A4,1 DRIVE 0 OR 1
0040	0034 F109	CFR	A1,A2 SELECT CASS DRIVE
0041	0036 0402	LDK	A4,2 LOCK CASS DRIVE
0042	0038 F109	CFR	A1,A2
0043	003A 0408	LDK	A4,8 SBOT SEARCH BEGIN OF TAPE
0044	003C F109	CFR	A1,A2
0045	003E 040C	LDK	A4,/C SIMF SEARCH TAPE MARK FORM
0046	0040 F109	CFR	A1,A2
0047	0042 040A	LDK	A4,/0A READ 1 BLOCK
0048	0044 570A	RF	READ
0049	0046 0403	LDK	A4,3 SEEK TO CYL 0
0050	0048 F109	CFR	A1,A2
0051	004A 7510	WER	A5,/10 IOP CW1
0052	004C 7611	WER	A6,/11 IOP CW2
0053	004E 040C	LDK	A4,/C READ SECTOR 3
0054	0050 F109	CFR	A1,A2
0055	0052 AF8C	QRR	A15,A3 PRESET REG A15
0056	0054 0F8A	AB	/B4 GOTO LOW CORE LOADER
0057	0056 44CB	CIO	CIO A4,1,/08 SUBROUTINE
0058	0058 4C0E	INR	INR A4,0,/0E READ DATA
0059	005A 5404	RF(4)	SST
0060	005C E439	SCR	A4,A6 STORE DATA IN MEMORY
0061	005E 1601	ADK	A6,1 INCREMENT MEMORY ADDRESS
0062	0060 4CC8	SST	SST A4,/08 STATUS?
0063	0062 5C0C	RB(4)	INR
0064	0064 87A0 63CB	LDKL	A15,/63CB LOAD A15
0065	0068 F024	RTN	A1
0066		* FLEX DISC PROGRAMMED CHANNEL	
0067	006A 0459	LDK	A4,/59 ADDR BIT 8-15 INR INSTR
0068	006C E331	SCR	A3,A4 MODIFY INR INSTR
0069	006E 045C	LDK	A4,/5C
0070	0070 B731	XRRS	A7,A4 CHANGE SCR IN STR INSTR
0071	0072 045E	LDK	A4,/5E
0072	0074 9031	IMR	A4 CHANGE ADK A6,1 IN ADK A6,2
0073		* FLEX DISC HARDWARE CHANNEL(MUX)	
0074	0076 7512	WER	A5,/12 IOP CW 1
0075	0078 7613	WER	A6,/13 IOP CW 2
0076	007A 8420 C020	LDKL	A4,/C020 READ 4 SEGMENT FROM SEGM 4
0077	007E 5F30	RB	READ
0078		END	START

# 1.1.14 CONTENTS IPL ROM B5300 (5131 194 35300/66)

DATE	82-03-06	IDENT	B5300
0000		IDENT	B5300
0001		*	DATE: 82 06 02 FOR PTS 0814/24
0002		*	FOR IPL FROM CASSETTE, FLEX DISC AND 2.5 AND 5M DISC
0003		*	AND BIG DISC
0004		*	CONTENTS OF A5 FOR SOP SWITCHES
0005		*SW1	/FE00 DCR DRIVE 0
0006		*SW2	/FD00 DCR DRIVE 1
0007		*SW3	/FC80 CARTRIDGE DISC DRIVE 0
0008		*SW4	/FC40 FIXED DISC DRIVE 0
0009		*SW5	/FC20 BIGD DRIVE 0
0010		*SW6	/FC10 BIGD DRIVE 1
0011		*SW7	/FC08 FLD DRIVE 0
0012		*SW8	/FC04 FLD DRIVE 1
0013		*SW9	/FC02 CARTRIDGE DISC DRIVE 1
0014		*SW10	/FC01 FIXED DISC DRIVE 1
0015			
0016	0000	57FE	START RF BEGIN
0017	0002	0680	LDK A6,/80 BASE ADDR LOW COR LOADER
0018	0004	EC20	0004 CWK A4,4 IS IT CASSETTE?
0019	0008	503A	RF(E) CASS
0020			*UPDATE DEVICE ADDRESS IN CIO AND SST
0021	000A	3C42	NOCASS SLL A4,2
0022	000C	9310	ADR A3,A4
0023	000E	E34C	0134 R LC A3,DA,A3 GET DEVICE PARAMETER
0024	0012	E329	SCR A3,A2 MODIFY CIO
0025	0014	E341	006D R SC A3,SST+1 MODIFY SST
0026	0018	1400	ADK A4,0 IS IT BIG DISC
0027	001A	5056	RF(E) BIGD
0028	001C	AB20	6300 NOBIGD DRKL A3,/6300 MAKE PARAMETER FOR A15 WITH DISC
0029	0020	0403	LDK A4,3 SEEK 0 COMMAND FOR FL1M AND DISC
0030	0022	F109	CFR A1,A2 DO SEEK 0 COMMAND
0031	0024	2710	ANK A7,/10 IF A7=/10 THEN IT IS NOT FL1M BUT FLO.25
0032	0026	545A	RF(NZ) FLO.25M
0033	0028	8720	5706 LDKL A7,/5706 LOAD RF(7) *18
0034	002C	8735	STR A7,A5 CHANGE INR INTO RF
0035	002E	A311	TM A3,A4 IS IT FL1MCU OR DISC
0036	0030	540C	RF(NZ) FL1MCU
0037	0032	040C	DISC LDK A4,/C FOR READ SECTOR 3
0038	0034	7110	WER A1,/10 FIRST CONTROL WORD IOP
0039	0036	7611	WER A6,/11 SECOND CONTROL WORD IOP
0040	0038	878C	LDR A15,A3 PARAMETER /63XX IN A15 (AS P800)
0041	003A	F109	READ READ LOW COR LOADER OR ELSE
0042	003C	0F84	AB /B4 START LOW CORE LOADER
0043	003E	0410	FL1MCU LDK A4,/10 READ FROM SECTOR 4
0044	0040	574C	RF CONT
0045	0042	5F0A	RB READ
0046	0044	E408	CASS ECR A4,A2
0047	0046	AC41	006B R ORS A4,STR CHANGE STR INSTR
0048	004A	840C	LDR A4,A3
0049	004C	2401	ANK A4,1 DRIVE 0 OR 1
0050	004E	F109	SEL CFR A1,A2 SELECT DRIVE
0051	0050	0402	LDK A4,2 LOCK
0052	0052	F109	LOCK CFR A1,A2 LOCK SEL CASS
0053	0054	0408	LDK A4,8 SEARCH BEGING OF TAPE
0054	0056	F109	SROT CFR A1,A2
0055	0058	040C	LDK A4,/C READ TAPE MARK
0056	005A	F109	STMF CFR A1,A2
0057	005C	040A	LDK A4,/A READ BLOCK
0058	005E	5F26	RB READ READ LOW CORE LOADER
0059	0060	0000	DATA 0
0060	0062	44CE	CIO A4,1,/0E START CONTROLLER
0061	0064	4F0E	INR INR A7,0,/0E READ CHAR OR WORD PC
0062	0066	5404	RF(NA) SST
0063	0068	8739	STR STR A7,A6 STORE CHAR OR WORD
0064	006A	1601	ADK A6,1 UPDATE ADDR
0065	006C	4FCE	SST A7,/0E ASK STATUS
0066	006E	5C0C	RB(NA) INR
0067	0070	F024	RTN A1
0068	0072	2701	BIGD ANK A7,1
0069	0074	3F44	SLL A7,4
0070	0076	851C	LDR A5,A7
0071	0078	AF41	012A R ORS A7,COMBIG+2
0072	007C	8420	012B R LDKL A4,COMBIG
0073	0080	5F48	RB READ
0074	0082	233F	FLO.25M ANK A3,/3F COMMAND BUFFER ADDR
0075	0084	E335	SCR A3,A5 READ SECTOR 0 FROM DISC
0076	0086	046A	LDK A4,/6A TAKE DEVICE ADDRESS
0077	0088	9031	INR A4 UPDATE INR INSTR
0078	008A	8420	C020 LDKL A4,/C020 UPDATE ADK A6,1 IN ADK A6,2
0079	008E	7112	WER A1,/12 READ 4 SEGMENTS FROM SEGM 4
0080	0090	7613	WER A6,/13 FIRST CONTROL WORD IOP
0081	0092	5F5A	RB READ SECOND CONTROL WORD IOP
			READ LOW CORE LOADER

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0082 0094 0000 0000          DATA      0,0,00,0,0,0,0,0,0
      0098 0000 0000
      009C 0000 0000
      00A0 0000 0000
      00A4 0000
0083 00A6 0000 0000          DATA      0,0,0,0,0,0,0,0,0
      00AA 0000 0000
      00AE 0000 0000
      00B2 0000 0000
      00B6 0000
0084 00B8 0000 0000          DATA      0,0,0,0,0,0,0,0,0
      00BC 0000 0000
      00C0 0000 0000
      00C4 0000 0000
      00C8 0000
0085 00CA 0000 0000          DATA      0,0,0,0,0,0,0,0,0
      00CE 0000 0000
      00D2 0000 0000
      00D6 0000 0000
      00DA 0000
0086 00DC 0000 0000          DATA      0,0,0,0,0,0,0,0,0
      00E0 0000 0000
      00E4 0000 0000
      00E8 0000 0000
      00EC 0000
0087 00EE 0000 0000          DATA      0,0,0,0,0,0,0,0,0
      00F2 0000 0000
      00F6 0000 0000
      00FE 0000
0088 0100 0263          BEGIN    LDK      A2,/63          ADDR CIO DA
0089 0102 8120 8100          LDKL     A1,/8100          FIRST CH IOP READ 256 WORDS
0090 0106 44EE          CIO        A4,1,/2E          START SOP
0091 0108 4D2E          READS     INR      A5,0,/2E          READ SOP SWITCH
0092 010A 5C04          RB(NA)    READS
0093 010C 3DB0          SRN        A5,A4          WHAT SW
0094 010E 9C11          NGR        A4,A4
0095 0110 1409          ADK        A4,9
0096 0112 E350 014E R          LC      A3,NUMB,A4
0097 0116 23FF          ANK        A3,/FF
0098 0118 E450 0144 R          LC      A4,NUM,A4
0099 011C 24FF          ANK        A4,/FF
0100 011E 43AE          CIO        A3,0,/2E          STOP SOP
0101 0120 4DC9          SST        A5,9          STATUS FLCU FLOPPY INSERTED AFTER IPL
0102 0122 0565          LDK        A5,/65          INR DA ADDR
0103 0124 870C          LDR        A7,A3
0104 0126 0F02          AR        2          BRANCH TO SORT
0105 0128 E000          COMBIG  DATA    /E000          SEEK TO 0
0106 012A 0800          DATA    /0800          READ SECTOR 0 HEAD 0
0107 012C 0180 0180          DATA    /180,/180          RECORD AND BLOCKLENGTH
0108 0130 0000 0000          DATA    /0000,/0000          BASE ADDRESS 0000
0109 0134 D7D7          DA        DATA    /D7D7          BIG DISC DRIVE 0
0110 0136 F7F7          DATA    /F7F7          BIG DISC DRIVE 1
0111 0138 C9D9          DATA    /C9D9          FIRST AND SEC FLD
0112 013A E9F9          DATA    /E9F9          THIRT AND FOURTH FLD
0113 013C C8E8          DATA    /C8E8          DRIVE 0 DISC CARTR AND FIXED
0114 013E D8F8          DATA    /D8F8          DRIVE 1 DISC
0115 0140 D7F7          DATA    /D7F7          BIG DISC DRIVE 0,1
0116 0142 0000          DATA    0
0117 0144 0404 0202          NUM      DATA    /0404,/0202,0,/0101,/0202
      0148 0000 0101
      014C 0202
0118 014E 0001 0001          NUMB     DATA    1,1,1,1,/203
      0152 0001 0001
      0156 0203
0119
0120
0121
0122          END      START

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#### SYMBOL TABLE

BEGIN	0100	R	BIGD	0072	R	CASS	0044	R	CIO	0062	R
COMBIG	0128	R	CONT	008E	R	DA	0134	R	DISC	0032	R
FLO25M	0082	R	FL1MCU	003E	R	INR	0064	R	LOCK	0052	R
NOBIGD	001C	R	NOCASS	000A	R	NUM	0144	R	NUMB	014E	R
READ	003A	R	READS	0108	R	SBOT	0056	R	SEL	004E	R
SORT	0002	R	SST	006C	R	START	0000	R	STMF	005A	R
STR	006B	R									

ASS.ERR. 0000

!EOF

PROG ELAPSED TIME: 00H-00M-34S-380MS-

# 1.1.15 CONTENTS IPL ROM BOOT 6A (5131 194 25900)

DATE	82-03-30	IDENT	BOOT6A	01-08-07	POHD
0000		IDENT	BOOT6A	01-08-07	POHD
0001					
0002					
0003		*	THIS BOOTSTRAP IS RELATED TO.		
0004		*	TSB 506/80 - BOOTSTRAP 64		
0005					
0006					
0007		*			
0008		*	B O O T S T R A P 6 0 0 0		
0009		*			
0010					
0011					
0012					
0013					
0014					
0015		*	SOP SWITCH 1 : CASSETTE UNIT 1		
0016		*	2 : UNIT 2		
0017					
0018		*	SOP SWITCH 3 : CARTRIDGE DISC 6875,6876		
0019		*	4 : FIXED DISC 6875,6876		
0020					
0021		*	SOP SWITCH 5 : BOMB DISC (OLD CU) UNIT 1		
0022		*	6 : UNIT 2		
0023					
0024		*	SOP SWITCH 7 : FLOPPY DISC UNIT 1 (ALL TYPES)		
0025		*	8 : UNIT 2 (ALL TYPES)		
0026					
0027		*	SOP SWITCH 9 : NOT USED		
0028		*	10 : NOT USED		
0029			EJECT		
0030	000E	CHCR	EGU /0E		
0031	002E	SOP	EGU /2E		
0032	0009	FDDA	EGU 9		
0033	0012	FDIOP	EGU /12		
0034	0010	DKIOP	EGU /10		
0035	0084	IPLSTA	EGU /84		
0036		*			
0037		*	READ SOP		
0038		*			
0039	0000	BOOT	EGU *		
0040	0000 0680	LDK	A6, /80		START ADDRESS OF IPL
0041	0002 0263	LDK	A2, S101+1-BOOT		SUBROUTINE ADDRESS
0042	0004 8120	LDKL	A1, /8100		WER REGISTER AND STACK ADDRESS
0043	0008 E308	ECR	A3, A2		A3: =/6300
0044	000A 44EE	CIO	A4, 1, SOP		
0045	000C 4D2E	INR	A5, 0, SOP		
0046	000E 5C04	RB(NA)	*-2		
0047	0010 44AE	CIO	A4, 0, SOP		
0048	0012 3DB0	SRN	A5, A4		
0049	0014 0565	LDK	A5, INRI+1-BOOT		ADDRESS TO INR INSTRUCTION
0050	0016 1C08	SUK	A4, 8		
0051	0018 5630	RF(NN)	CASS		TAPE CASSETTE
0052	001A E350	LC	A3, DEVADR-BOOT, A4		DEVICE ADDRESS
0053	001E E329	SCR	A3, A2		UPDATE ADDRESS IN CIO
0054	0020 6341	SC	A3, SSTI+1-BOOT		UPDATE ADDRESS IN SST
0055		EJECT			
0056		*			
0057		*			
0058		*	DISC		
0059	0024	DISC	EGU *		
0060	0024 0403	LDK	A4, 3		
0061	0026 F109	CFR	A1, A2		SEEK ZERO
0062	0028 2710	ANK	A7, /10		
0063	002A 5446	RF(NZ)	FDPC		0.25 MEG FLOPPY DRIVE
0064	002C A311	TH	A3, A4		
0065	002E 5410	RF(NZ)	FD1M		1 MEG FLOPPY
0066	0030 040C	LDK	A4, /C		SECTOR 3
0067	0032 7110	WER	A1, DKIOP		
0068	0034 7611	WER	A6, DKIOP+1		BUFFER ADDRESS
0069	0036 878C	LDR	A15, A3		PARAMETER TO IPL
0070	0038 570C	RF	EXIT		
0071		EJECT			
0072	003A D9C9	DATA	/D9C9		SOP SWITCH 8, 7
0073	003C F7D7	DATA	/F7D7		SOP SWITCH 6, 5
0074	003E EBC8	DATA	/EBC8		SOP SWITCH 4, 3
0075	0040	DEVADR	EGU *		
0076		EJECT			
0077		*			
0078		*	1 MEGABYTE FLOPPY		
0079		*			
0080	0040	FD1M	EGU *		
0081	0040 0410	LDK	A4, /10		FIRST SECTOR TO READ=2
0082	0042	FDWER	EGU *		
0083	0042 7112	WER	A1, FDIOP		
0084	0044 7613	WER	A6, FDIOP+1		BUFFER ADDRESS

DATE 82-03-30 IDENT BOOT6A 81-08-07 P0HD

```

0085          EJECT
0086          *
0087          *   EXIT
0088          *
0089          0046      EXIT   EQU      *
0090 0046 F109      CFR      A1,A2      READ
0091 004B 0F84      AB       IPLSTA      GO TO IPL
0092          *
0093          *   EXIT TO IPLSTA
0094          *
0095          *   TAPE CASSETTE      A4=/000A
0096          *   BRANCH TO ADDRESS /42 IN BOOTSTARP FROM CASSETTE IPL,A4 UNCHANGED
0097          *
0098          *   PTS 6875 FIXED DISC      A15=/63EB
0099          *   PTS 6875 CARTRIDGE DISC  A15=/63CB
0100          *
0101          *   FLOPPY DISC 1 P.C      A3=/0009
0102          *   FLOPPY DISC 2 P.C      A3=/0019
0103          *   1 MEGABYTE FLOPPY DISC 1  A3=/XXC9
0104          *   1 MEGABYTE FLOPPY DISC 2  A3=/XXD9
0105          *   EJECT
0106          *
0107          *   CASSETTE
0108          *
0109          004A      CASS   EQU      *
0110 004A AB41 006B   OPS      A3,SCRI-BOOT      STR CHANGED TO SCR IN READ ROUTINE
0111 004E 3401      XRR      A4,1      SELECT CASSETTE
0112 0050 F109      CFR      A1,A2
0113 0052 0402      LDK      A4,2      LOAD
0114 0054 F109      CFR      A1,A2
0115 0056 040B      LDK      A4,B      SEARCH BOT
0116 005B F109      CFR      A1,A2
0117 005A 040C      LDK      A4,/C      SEARCH TAPE MARK
0118 005C F109      CFR      A1,A2
0119 005E 040A      LDK      A4,/A      READ ONE BLOCK
0120 0060 5F1C      RB       EXIT
0121          *   EJECT
0122          *
0123          *   SUBROUTINE TO READ
0124          *
0125          0062      SIQI   EQU      *
0126 0062 44CE      CIO      A4,1,CHCR
0127 0064      INRI   EQU      *
0128 0064 4F0E      INR      A7,0,CHCR
0129 0066 5404      RF(NA)   SSTI
0130 006B      SCRI   EQU      *
0131 006B B739      STR      A7,A6
0132 006A      ADKI   EQU      *
0133 006A 1601      ADK      A6,1
0134 006C      SSTI   EQU      *
0135 006C 4FCE      SSI      A7,CHCR
0136 006E 5C0C      RB(NA)   INRI
0137 0070 F024      RTN      A1
0138          *   EJECT
0139          *
0140          *   FLOPPY DISC
0141          *
0142          0072      FDPC   EQU      *
0143 0072 233F      ANK      A3,/3F
0144 0074 E335      SCR      A3,A5      UPDATE ADDRESS IN INR INSTRUCTION
0145 0076 046A      LDK      A4,ADKI-BOOT
0146 007B 9031      IMR      A4      CHANGE TO ADK A6,2
0147 007A 8420 C020  LDKL     A4,/C020  4 PHYS. SECTORS A 128 BYTES,START IN SEC
0148 007E 5F3E      RB       FDWER
0149          *
0150          *
0151          0080      BOOTEND EQU      *
0152          *   END      BOOT

```

# SYMBOL TABLE

ADKI	006A	R	BOOT	0000	R	BOOTEND	0080	R	CASS	004A	R
CHCR	000E	A	DEVADR	0040	R	DISC	0024	R	DKIOP	0010	A
EXIT	0046	R	FDIM	0040	R	FDDA	0009	A	FDIOP	0012	A
FDPC	0072	R	FDWER	0042	R	INRI	0064	R	IPLSTA	0084	A
SCRI	006B	R	SIQI	0062	R	SOP	002E	A	SSTI	006C	R

ASS ERR. 0000

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 PROG ELAPSED TIME. 00H-00M-22S-640MS-

# 1.1.16 CONTENTS IPL ROM BOOT 6C (5131 194 41700)

DATE	B2-03-30	IDENT	BOOT6C	81-10-07	POHO
0000		IDENT	BOOT6C	81-10-07	POHO
0001					
0002					
0003		*	THIS BOOTSTRAP IS RELATED TO		
0004		*	TSB 506/B0 - BOOTSTRAP 65		
0005					
0006					
0007		*			
0008		*	B O O T S T R A P 6 0 0 0		
0009		*			
0010					
0011					
0012					
0013					
0014					
0015		*	SOP SWITCH 1	CARTRIDGE 16MB OR 80MB UNIT 1	
0016		*	2	FIXED 16MB DISC UNIT 1	
0017					
0018		*	SOP SWITCH 3 :	CARTRIDGE DISC 6875.6876	
0019		*	4 :	FIXED DISC 6875.6876	
0020					
0021		*	SOP SWITCH 5 :	CARTRIDGE DISC 6875.6876 UNIT 2	
0022		*	6 :	FIXED DISC 6875.6876 UNIT 2	
0023					
0024		*	SOP SWITCH 7	FLOPPY DISC UNIT 1 (ALL TYPES)	
0025		*	8 :	UNIT 2 (ALL TYPES)	
0026					
0027		*	SOP SWITCH 9 :	NOT USED	
0028		*	10 :	NOT USED	
0029			EJECT		
0030	000E	CHCR	EGU	/0E	
0031	002E	SDP	EGU	/2E	
0032	0007	FDDA	EGU	9	
0033	0012	FDIOP	EGU	/12	
0034	0010	DKIOP	EGU	/10	
0035	0084	IPLSTA	EGU	/84	
0036		*			
0037		*	READ SOP		
0038		*			
0039	0000	BOOT	EGU	*	
0040	0000 0680	LDK	A6./B0		START ADDRESS OF IPL
0041	0002 0263	LDK	A2,SIOI+1-BOOT		SUBROUTINE ADDRESS
0042	0004 B120 B100	LDKL	A1./B100		WER REGISTER AND STACK ADDRESS
0043	0008 E308	ECR	A3.A2		A3 =/6200
0044	000A 44EE	CIO	A4.1,SDP		
0045	000C 4D2E	INR	A5.0,SDP		
0046	000E 5C04	RB(NA)	*-2		
0047	0010 44AE	CIO	A4.0,SDP		
0048	0012 3DB0	SRN	A5.A4		
0049	0014 0565	LDK	A5,INRI+1-BOOT		ADDRESS TO INR INSTRUCTION
0050	0016 E350 0048	LC	A3.DEVADR-BOOT.A4		DEVICE ADDRESS
0051	001A E329	SCR	A3.A2		UPDATE ADDRESS IN CIO
0052	001C E341 006D	SC	A3,SSTI+1-BOOT		UPDATE ADDRESS IN SST
0053	0020 1C07	SUK	A4.7		
0054	0022 512E	RF(P)	CDDISC		16M OR 80M DISC
0055		EJECT			
0056		*			
0057		*	DISC		
0058		*			
0059	0024	DISC	EGU	*	
0060	0024 0403	LDK	A4.3		
0061	0026 F109	CFR	A1.A2		SEEK ZERO
0062	0028 2710	ANK	A7./10		
0063	002A 5446	RF(NZ)	FDPC		0.25 MEG FLOPPY DRIVE
0064	002C A311	TM	A3.A4		
0065	002E 540A	RF(NZ)	FDIM		1 MEG FLOPPY
0066	0030 040C	LDK	A4./C		SECTOR 3
0067	0032 7110	WER	A1,DKIOP		
0068	0034 7611	WER	A6,DKIOP+1		BUFFER ADDRESS
0069	0036 878C	LDR	A15.A3		PARAMETER TO IPL
0070	0038 5724	RF	EXIT		
0071		EJECT			
0072		*			
0073		*	1 MEGABYTE FLOPPY		
0074		*			
0075	003A	FDIM	EGU	*	
0076	003A 0410	LDK	A4./10		FIRST SECTOR TO READ=2
0077	003C 573C	RF	FDWER		



```

0078          EJECT
0079          *
0080          *      READ TABLE FOR 16M AND 80M DISC
0081          *
0082
0083          003E      SEEK      EQU      *
0084          003E E000      DATA    /E000      SEEK TO ZERO
0085          0040      READ12    EQU      *
0086          0040 0800      DATA    /0800      READ LOGICAL SECTOR 0.1 AND 2
0087          0042 0180      DATA    /0180      TOTAL LENGTH
0088          0044 0180      DATA    /0180      NO TRANSFER LOG. SEC. 0
0089          0046 0000 0000      DATA    0.0      DUMMY ADDRESS
0090          EJECT
0091          0048      DEVADR    EQU      *-2
0092          004A D9C9      DATA    /D9C9      SOP SWITCH B.7
0093          004C FBDB      DATA    /FBDB      SOP SWITCH 6.5
0094          004E EBCB      DATA    /EBCB      SOP SWITCH 4.3
0095          0050 D7D7      DATA    /D7D7      SOP SWITCH 2.1
0096          EJECT
0097          *
0098          *      16M OR 80M DISC
0099          *
0100          0052      CDDISC    EQU      *
0101          0052 2401      ANK      A4.1
0102          0054 3C44      SLL      A4.4      BIT IN POSITION DEVICE NUMBER
0103          0056 8510      LDR      A5,A4      FIX OR CARTRIDGE
0104          0058 AC41 0040      ORS      A4,READ12-BOOT      SET DEVICE NUMBER BIT
0105          005C 043E      LDK      A4,SEEK-BOOT
0106          EJECT
0107          *
0108          *      EXIT
0109          *
0110          005E      EXIT      EQU      *
0111          005E F109      CFR      A1,A2      READ
0112          0060 0FB4      AB      IPLSTA      GO TO IPL
0113          *
0114          *      EXIT TO IPLSTA
0115          *
0116          *      TAPE CASSETTE      A4=/000A
0117          *      BRANCH TO ADDRESS /42 IN BOOTSTARP FROM CASSETTE IPL,A4 UNCHANGED
0118          *
0119          *      PTS 6875 FIXED DISC      A15=/63EB
0120          *      PTS 6875 CARTRIDGE DISC      A15=/63CB
0121          *
0122          *      FLOPPY DISC 1 P C      A3=/0009
0123          *      FLOPPY DISC 2 P C      A3=/0019
0124          *      1 MEGABYTE FLOPPY DISC 1      A3=/XXC9
0125          *      1 MEGABYTE FLOPPY DISC 2      A3=/XXD9
0126          EJECT
0127          *
0128          *      SUBROUTINE TO READ
0129          *
0130          0062      SIOI      EQU      *
0131          0062 44CE      CIO      A4.1,CHCR
0132          0064      INRI      EQU      *
0133          0064 4F0E      INR      A7.0,CHCR
0134          0066 5404      RF(NA)    SSTI
0135          0068      SCRI      EQU      *
0136          006B 8739      STR      A7,A6
0137          006A      ADKI      EQU      *
0138          006A 1602      ADK      A6.2
0139          006C      SSTI      EQU      *
0140          006C 4FCE      SST      A7,CHCR
0141          006E 5C0C      RB(NA)    INRI
0142          0070 F024      RTN      A1
0143          EJECT
0144          *
0145          *      FLOPPY DISC
0146          *
0147          0072      FDPC      EQU      *
0148          0072 233F      ANK      A3./3F
0149          0074 E335      SCR      A3,A5      UPDATE ADDRESS IN INR INSTRUCTION
0150          0076 8420 C020      LDKL    A4./C020      4 PHYS. SECTORS A 128 BYTES, START IN SEC
0151          007A      FDWER      EQU      *
0152          007A 7112      WER      A1,FDIOP
0153          007C 7613      WER      A6,FDIOP+1      BUFFER ADDRESS
0154          007E 5F22      RB      EXIT
0155
0156
0157          0080      BOOTEND    EQU      *
0158          END      BOOT

```

## SYMBOL TABLE

ADKI	006A	R	BOOT	0000	R	BOOTEND	0080	R	CDDISC	0052	R
CHCR	000E	A	DEVADR	0048	R	DISC	0024	R	DKIOP	0010	A
EXIT	005E	R	FDIM	003A	R	FDDA	0009	A	FDIOP	0012	A
FDPC	0072	R	FDWER	007A	R	INRI	0064	R	IPLSTA	0084	A
READ12	0040	R	SCRI	006B	R	SEEK	003E	R	SIOI	0062	R
SOP	002E	A	SSTI	006C	R						

ASS. ERR. 0000

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 PROG ELAPSED TIME 00H-00M-23S-820MS~



## 1.2 EXTERNAL CONNECTIONS

### 1.2.1 Compatibility between Computers

All interface units described in this section are hardware - compatible with all computers covered by this manual. With other words; all interface units can, from a **HARDWARE** point of view, be used in any of the computers 6810-6814 and 6824. Interface units that are classified as masters should, as far as possible, be located in the computer cabinet of an extended system. However, when required, it is now allowed to locate masters in extension cabinets of type 6864.

### 1.2.2 Star-Connected Work Stations

#### Definition of Star Network

Figure 1.2-1

A star network is defined as an interconnecting system where a number of external points (in this case; work stations) are connected to a central junction (computer interface unit) **VIA SEPARATE LINES**, see Figure 1.2-1. This method of connecting work stations to computers is well-known from earlier PTS 6000 installations.

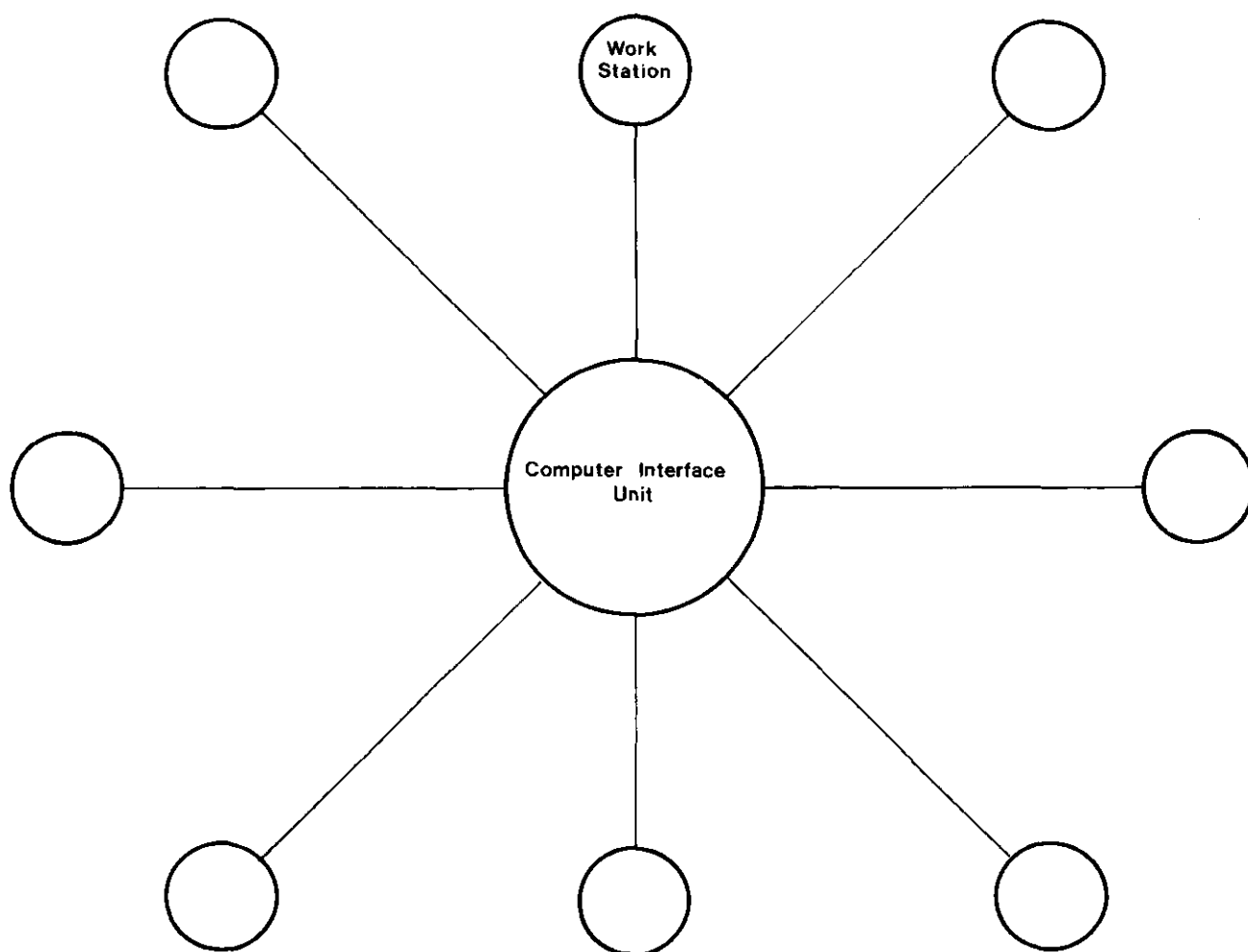


Figure 1.2-1 Definition of Star Network

## Local Work Stations

Figure 1.2-2

Up to eight local work stations can be connected via the computer interface unit CHLT 6831, located in a computer or an extension cabinet. The lines exit via eight plugs, vertically fitted at the front edge of the CHLT. These plugs are addressed as Terminal 0-7, from bottom to top. The system is prepared for having two CHLTs, (enabling the connection of 16 local work stations), but the number of CHLTs can be extended to four.

Figure 1.2-2 shows three different work stations connected to the CHLT. These work stations have been chosen with the purpose to indicate the development towards more and more compact work station units.

Work stations of earlier generations (terminal 0 in figure) had a separate communication unit (SUML) to which various I/O devices could be connected. In later generations of work stations (terminal 1 and 2 in figure) the communication part has been integrated in one of the I/O devices (TEP 6371/72) or together with several I/O devices in a compact desk top work station unit (CFT 6281/83).

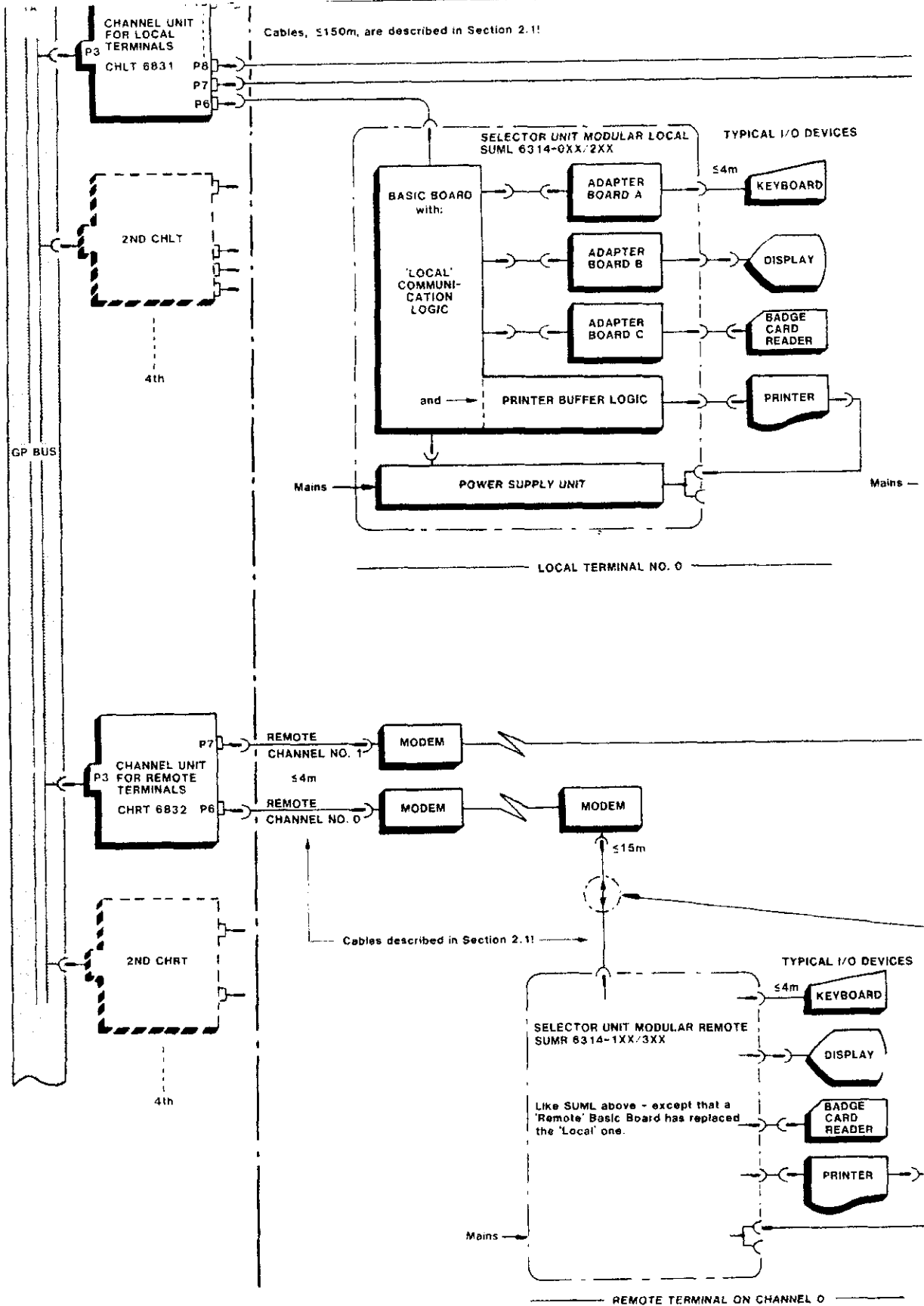
## Remote Work Stations

Figure 1.2-2

One or two remote channels can be connected via the computer interface unit CHRT 6832, located in a computer or an extension cabinet. The channels exit via two plugs at the front edge of the CHRT; the bottom one being addressed as channel 0 and the top one as channel 1. The system is prepared for having two CHRTs, (enabling the connection of four remote channels), but the number of CHRTs can be extended to four.

Each channel is routed via a local modem, a telephone line and a remote modem to the remote work station. A remote work station of an earlier generation (on channel 0 in figure) is equipped with a separate communication unit (SUMR), similar to the local work station of the same generation. Remote work stations of later generations have the communication part integrated in one of the I/O devices, e.g. in a TEP 6371/72 as shown on channel 1.

The number of connectable work stations can be doubled if TFUs are used at the remote sites. Each TFU, connected after the remote modem, enables the connection of two work stations to each channel.





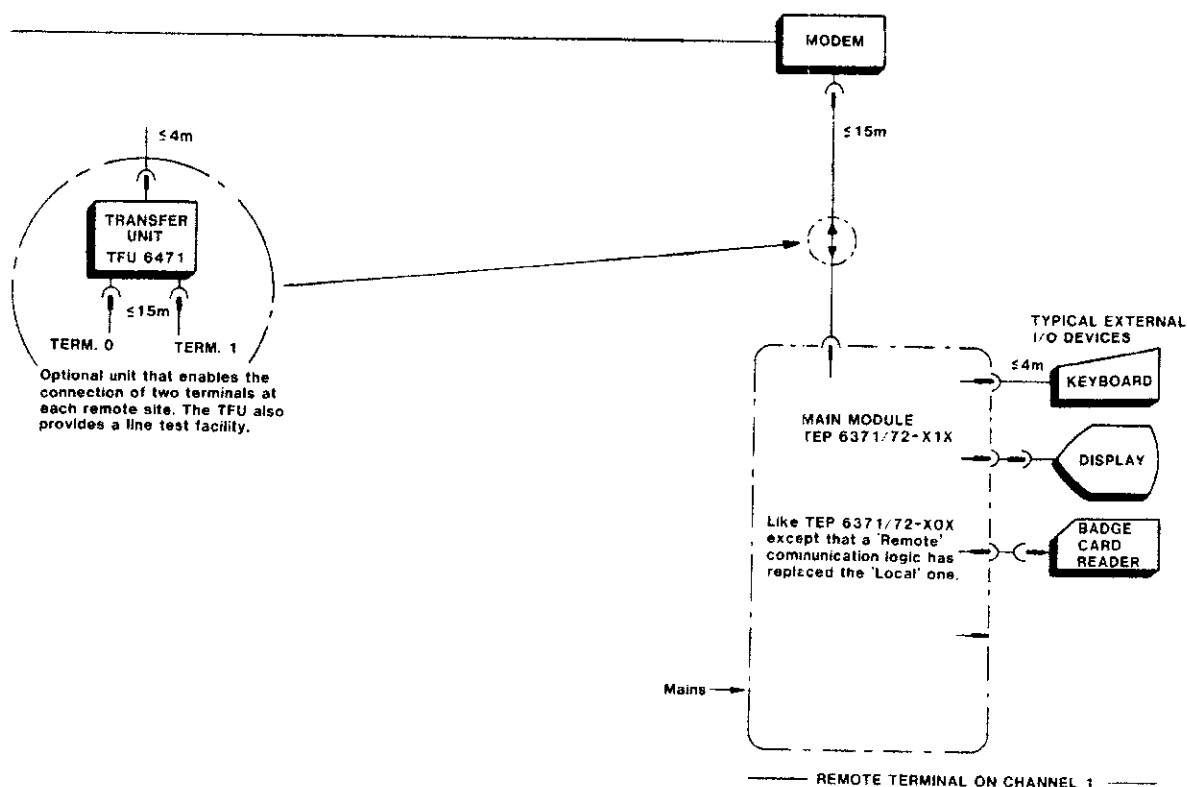
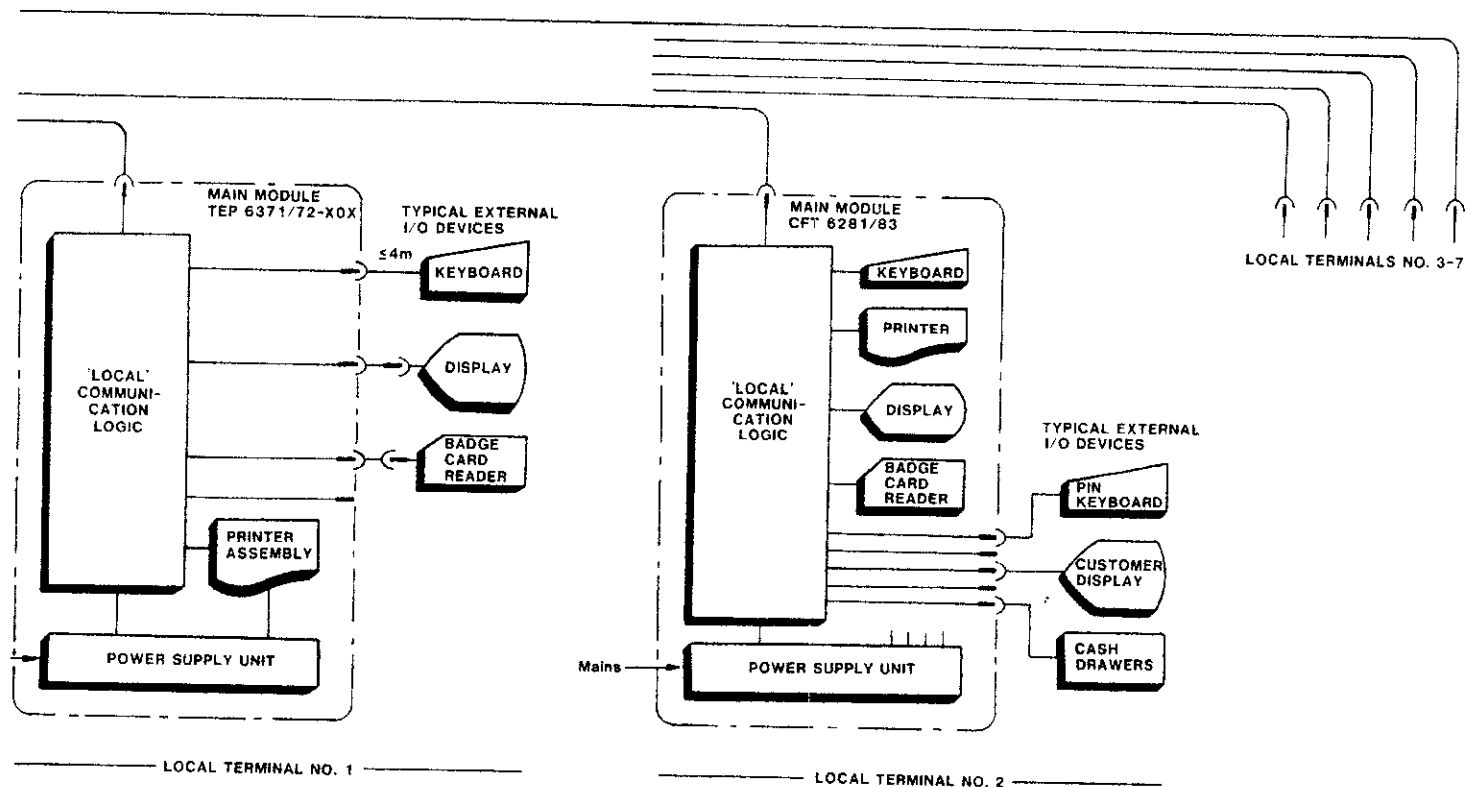


Figure 1.2-2 Star-Connected Work Stations





### 1.2.3 Multidrop-Connected Work Stations

#### Definition of Multidrop Network

Figure 1.2-3

A multidrop network is defined as an interconnecting system where a number of external points (in this case; work stations) are connected to a central junction (computer interface unit) VIA A SINGLE LINE, see Figure 1.2-3. This method of connecting work stations, that will replace the former star method, has been introduced to increase the capacity and the reliability of the data transfers.

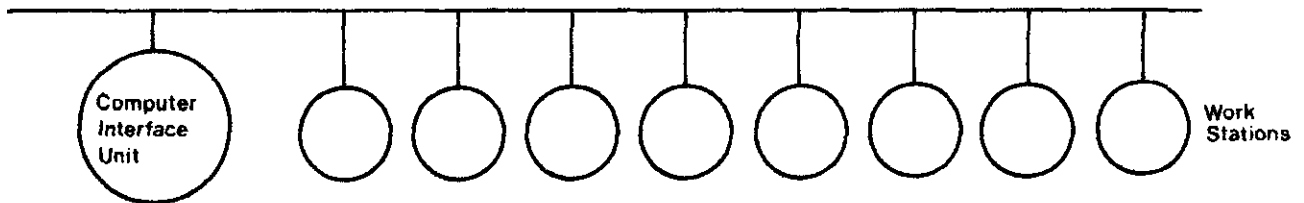


Figure 1.2-3 Definition of Multidrop Network

#### Local Work Stations

Figure 1.2-4

Up to 32 work stations can be connected to the single multidrop line that is controlled by the computer interface unit CHLW 6895. However, in typical applications the number of work stations is limited to 6-8, due to performance reasons. The CHLW is classified as a master and should, if possible, be located in the computer cabinet (in TC 6810/11 systems it is absolutely necessary). The line exits via a plug at the front edge of the CHLW and can have a maximum length of 750 m. When being necessary the system can be equipped with more than one CHLW, up to a maximum of four.

A work station connected to the multidrop line has usually an I/O device that includes the necessary communication interface, a Local Work Station Interface (LWSI). Such a device is known as the main module of the work station, and interconnects itself and other I/O devices with the multidrop line. Figure 1.2-4 shows the most common main modules.

A work station without any I/O main module is connected via a separate main module, a Modular Device Adapter - MDA 6411. The system function of this main module is similar to the former SUMLS; a communication interface interconnects line and I/O devices via adapter boards, and a power supply unit provides the necessary D.C. supply.

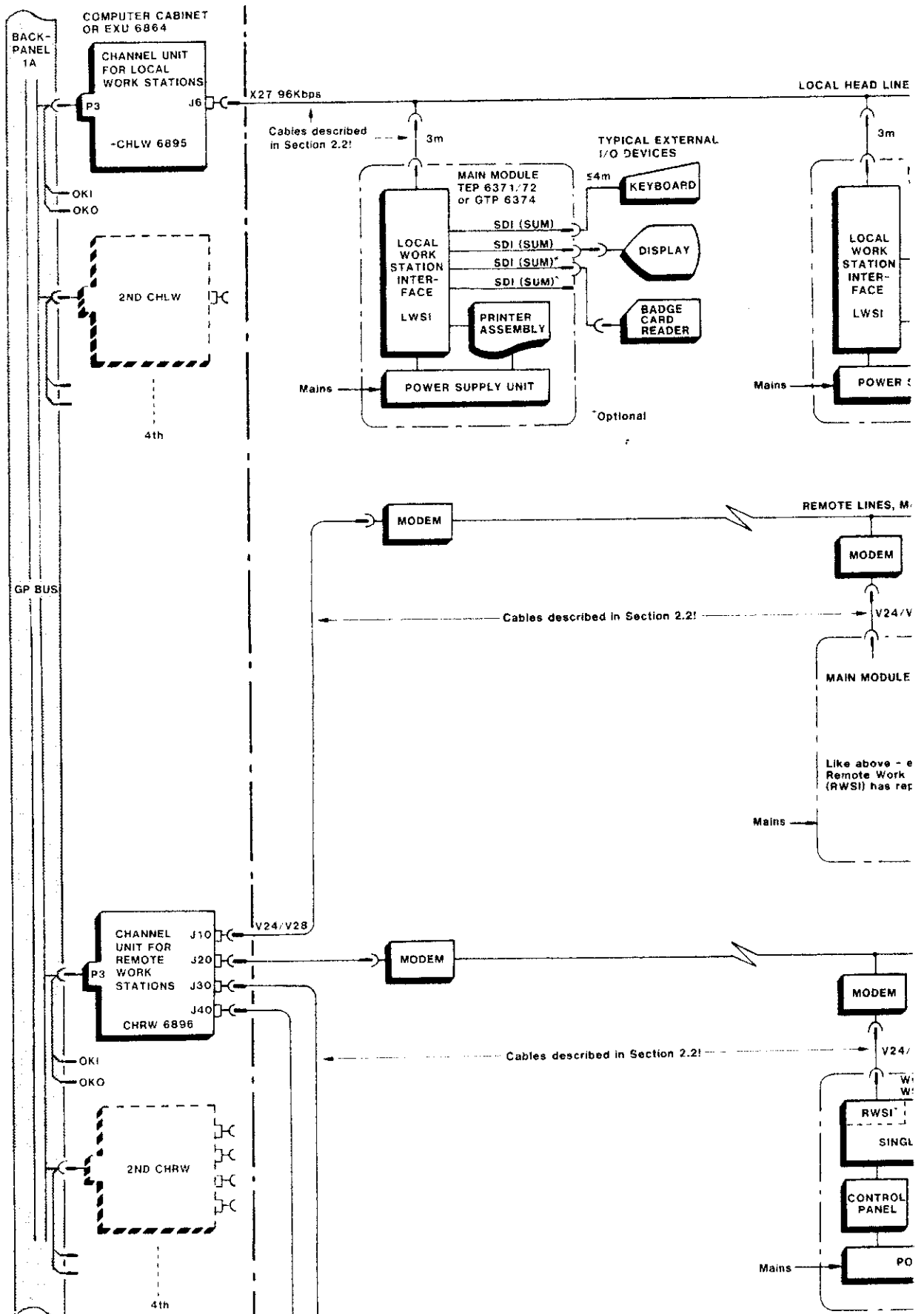
#### Remote Work Stations

Figure 1.2-4

Up to four remote multidrop lines can be controlled by the computer interface unit CHRW 6896. This unit is classified as a master and should, if possible, be located in the computer cabinet (in TC 6810/11 systems it is absolutely necessary). The lines exit via four plugs at the front edge of the CHRW, the top one being addressed as line 0 and the bottom one as line 3. Line 0 can also be used for computer-to-computer communications. When being necessary the system can be equipped with more than one CHRW, up to a maximum of four.

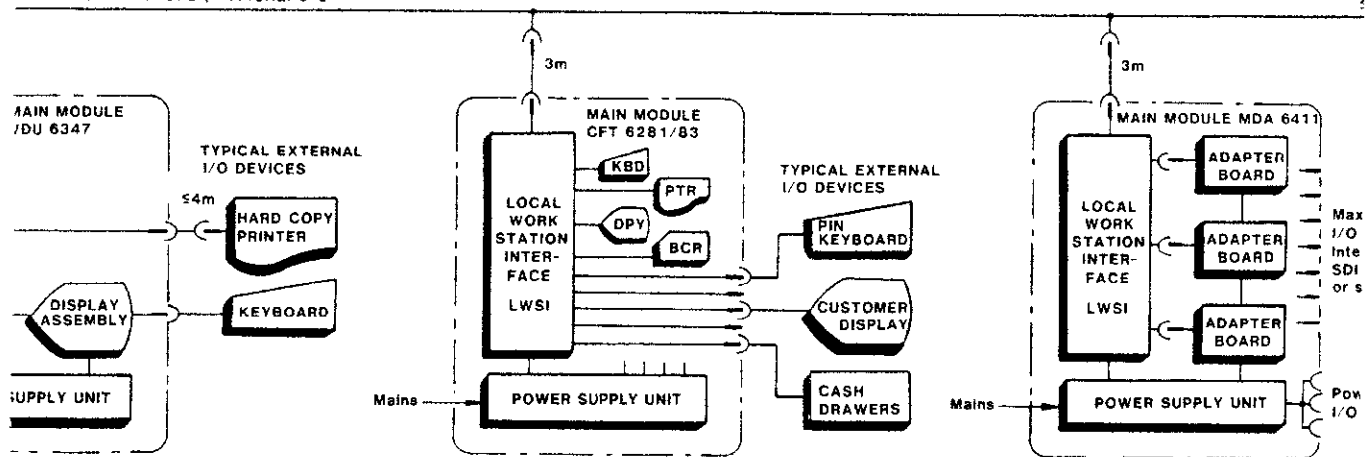
Each line enters the PTT domain via a local modem that leads to a leased line. Up to eight drops are allowed on each line, either to single work stations or to work station controllers. However, in typical applications the number of drops is limited to 2-3, due to performance reasons.







- MAX. OF 32 DROPS, TYPICAL: 6-8



1X. OF 8 DROPS/LINE, TYPICAL: 2-3

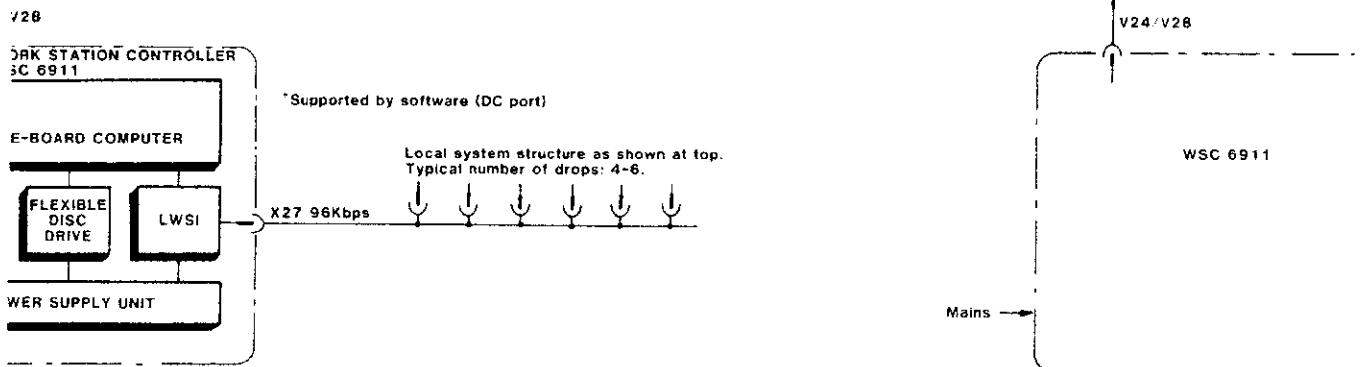
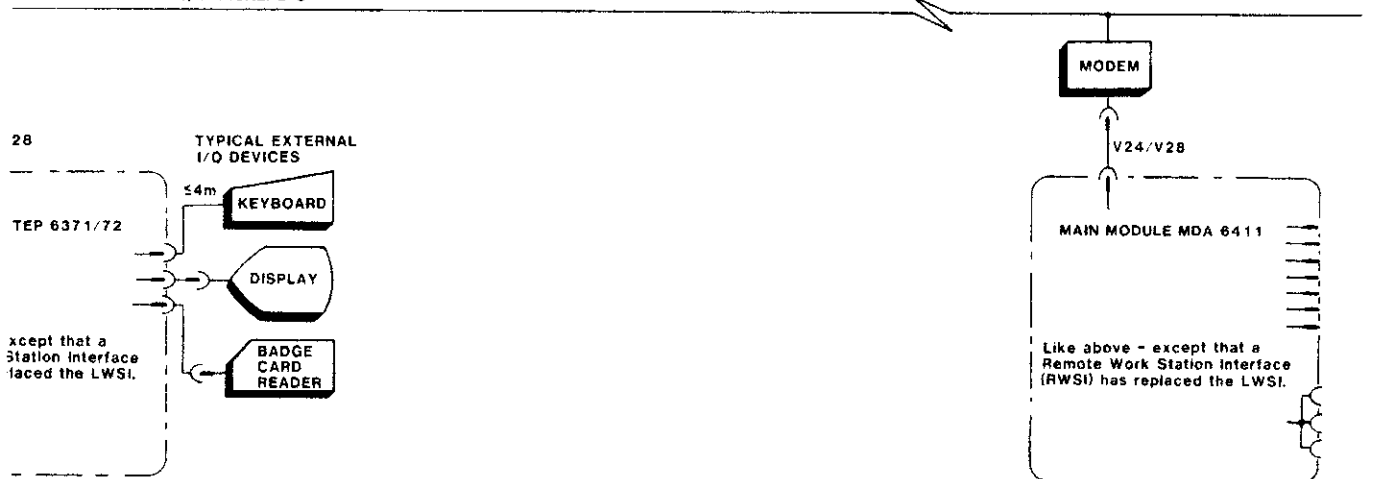


Figure 1.2-4 Multidrop-Connected Work Sta



A single work station has usually an I/O device that is classified as a main module, i.e. it includes the necessary communication interface; in this case a Remote Work Station Interface (RWSI). This interface connects the 'own' and other I/O devices to the line via a remote modem. A single work station without any I/O main module is connected via a separate main module, an MDA 6411 that is now equipped with an RWSI (compare with local work stations).

A work station controller is a small computer that can be used for converting a remote drop (via RWSI) into a local structure that is controlled via LWSI. This local structure is (except for performance) equivalent to the one controlled by CHLW at the site of the terminal computer.

#### 1.2.4 Connection of Peripherals

##### Console Typewriter CTW 6862

Figure 1.2-5

A console typewriter of type 6862 can be connected to an interface circuit that is contained on the computers' CPU board. In the computers 6810-6812 (CPU P852) this interface operates according to the Current Loop method. The CTW must then be equipped with the same type of interface and is connected via a 2-wire cable (signal and ground) to fast-on pins on backpanel 1B.

An upgraded 6810/11 or computers of type 6813, 6814 or 6824 (CPU P857, P857R, P857RA) have instead a V24 interface. A CTW equipped with the same type of interface can then be connected via P7 on backpanel 1B.

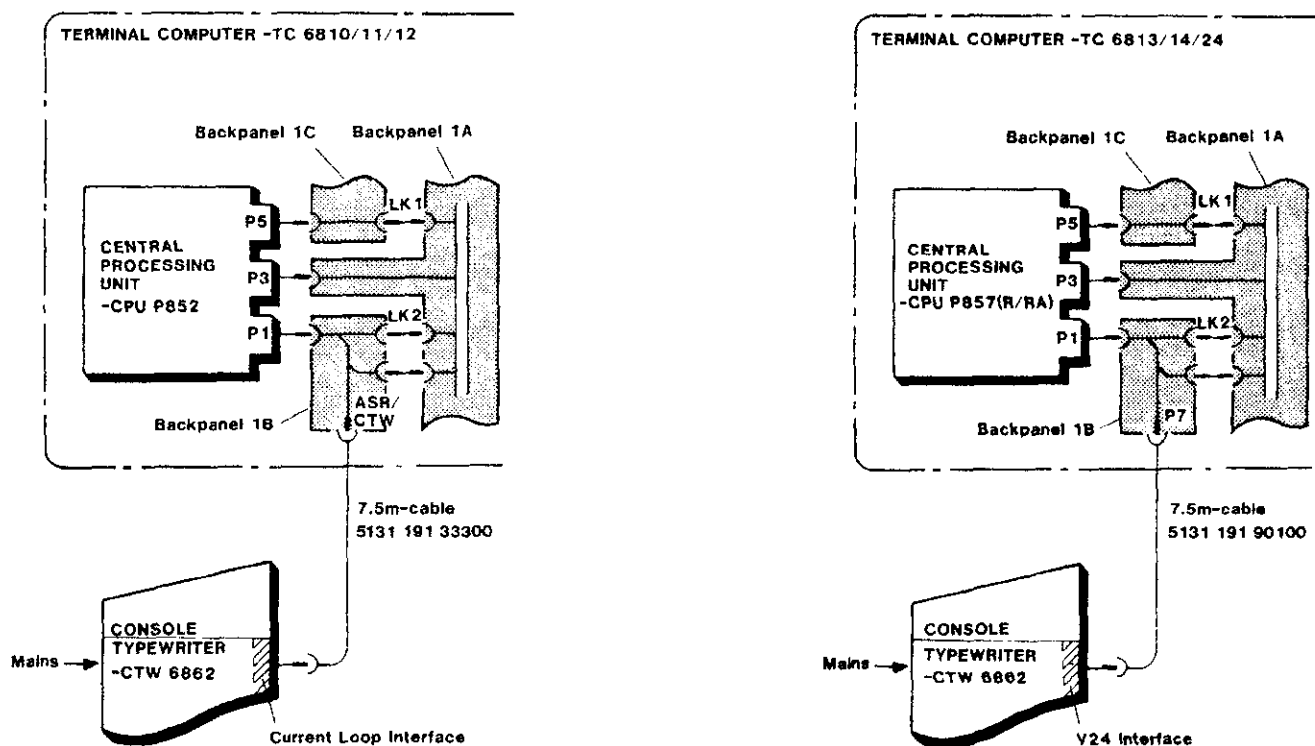


Figure 1.2-5 Connection of Console Typewriter





## Flexible Disc Unit FDU 6879

Figure 1.2-6

An external flexible disc unit of type 6879 (primarily intended for TC 6810/11) can be controlled via the computer interface unit CHFD 6848. The FDU can be equipped with one or two flexible disc drives of type 6867 (each of 250 Kbytes) and is connected via two cables to front edge connectors on the CHFD.

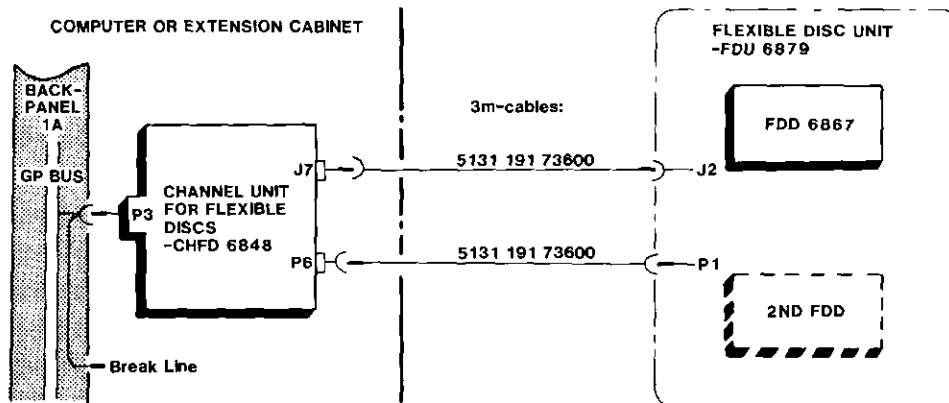


Figure 1.2-6 Connection of Flexible Disc Unit

## Cartridge Disc Unit CDU 6875/76

Figure 1.2-7

Up to two cartridge disc units of type 6875/76 (2x3.1 Mbytes/2x6.25 Mbytes) can be controlled via the computer interface unit CHDU 6844. The CDUs are connected to the CHDU via two separate cables, terminated with sockets that are fixed to the rack for accepting the edge plugs P1 and P5 of the CHDU.

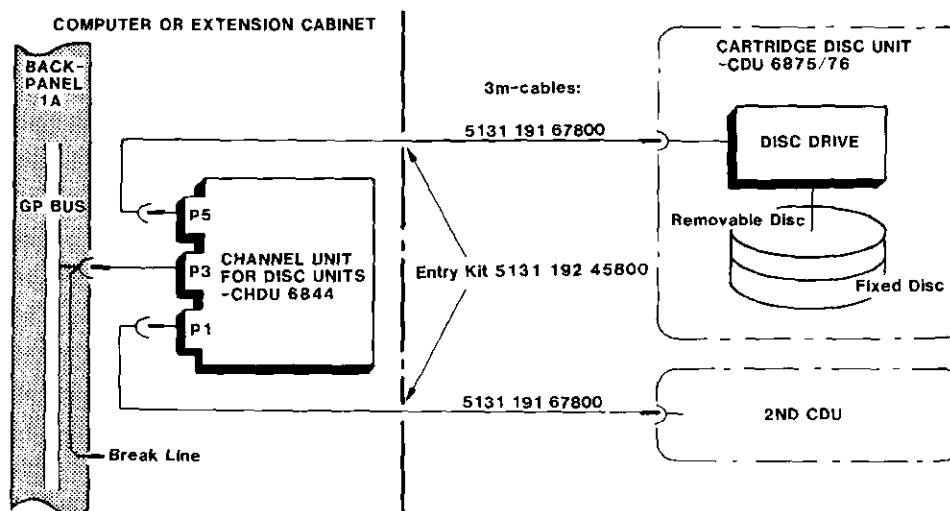


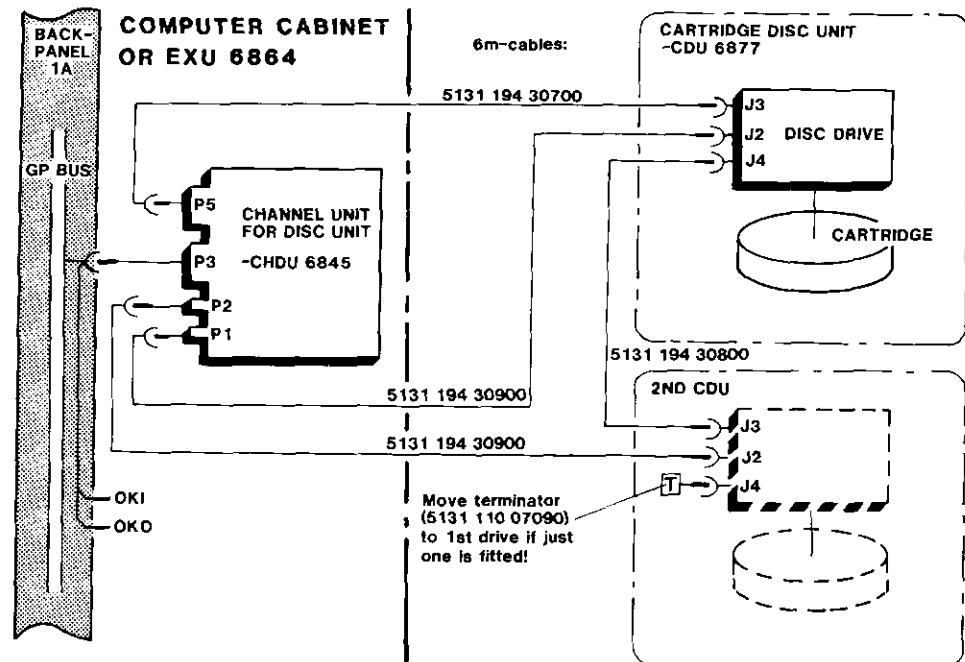
Figure 1.2-7 Connection of Cartridge Disc Unit(s), type 6875/76

## Cartridge Disc Unit CDU 6877

Figure 1.2-8

One or two cartridge disc units of type 6877 (80 Mbytes) can be controlled via the computer interface unit CHDU 6845. This unit is classified as a master and should, if possible, be located in the computer cabinet (in TC 6810/11 systems it is absolutely necessary). The CDUs are connected via cables that are terminated with sockets, fixed to the rack for accepting the edge plugs P1, P2 and P5 of the CHDU.

Figure 1.2-8  
Connection of  
Cartridge Disc  
Unit(s), type  
6877

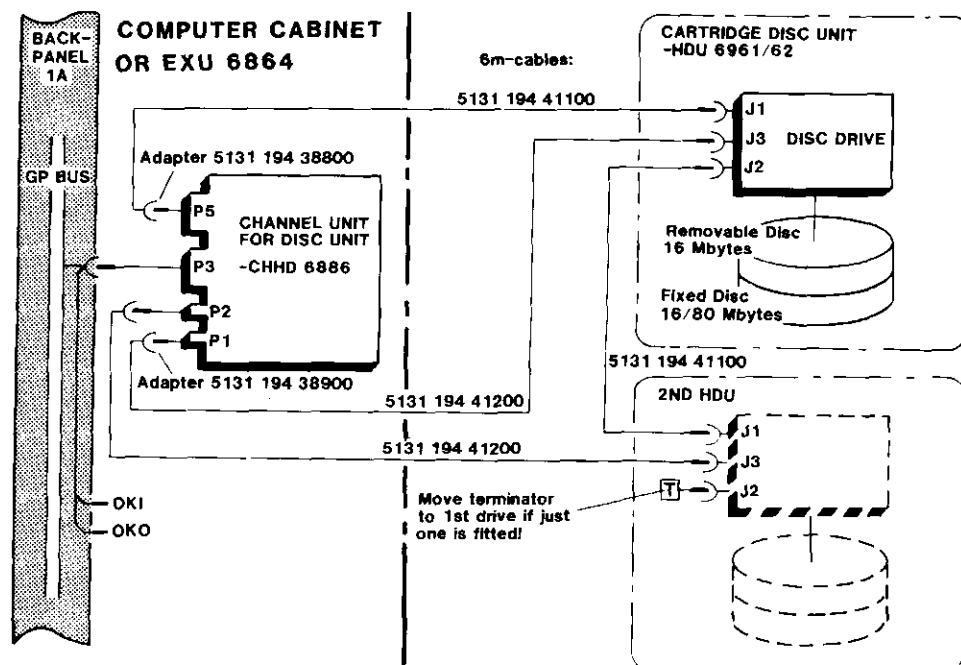


## Cartridge Disc Unit HDU 6961/62

Figure 1.2-9

Up to two cartridge disc units of type 6961/62 (16+16 Mbytes/16+80 Mbytes) can be controlled via the computer interface unit CHHD 6886. This unit is classified as a master and should, if possible, be located in the computer cabinet (in TC 6810/11 systems it is absolutely necessary). The HDUs are connected via cables that are terminated with sockets, fixed to the rack for accepting the edge plugs P1, P2 and P5 of the CHHD.

Figure 1.2-9  
Connection of  
Cartridge Disc  
Unit(s), type  
6961/6962



**Matrix Line Printer MLP 6881/82  
Card Reader CRD 6885**

Figure 1.2-10

A matrix line printer of type 6881/82 (200/400 lpm) and a card reader of type 6885 can both be controlled via the computer interface unit CHCD 6847. Both units are connected via cables that are terminated with sockets, fixed to the rack for accepting the CHCD's edge plugs P1, P2 (CRD cable) and P4, P5 (MLP cable).

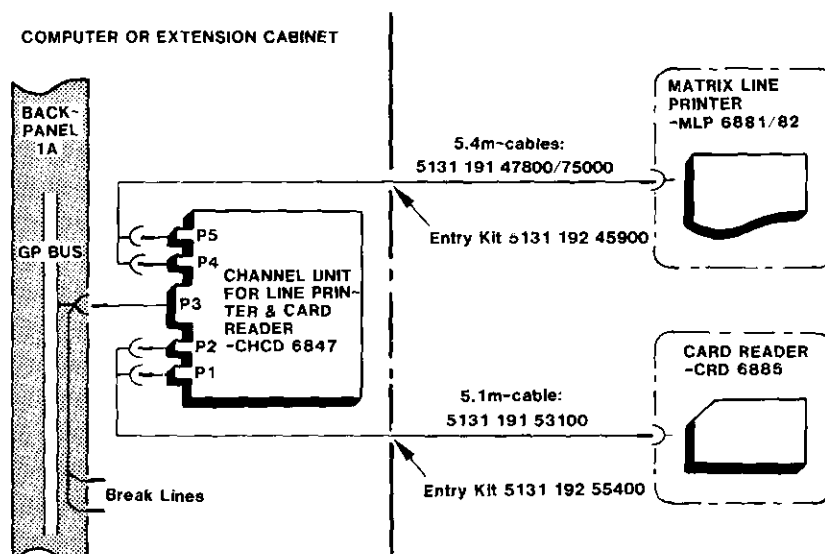


Figure 1.2-10 Connection of Matrix Line Printer and Card Reader

**Magnetic Tape Unit MTU 6872**

Figure 1.2-11

A magnetic tape unit of type 6872 can be controlled via the computer interface unit CHMT 6842. The tape unit is connected via four cables to front edge plugs on the CHMT. When required it is possible to connect a second MTU-cabinet with another tape transport.

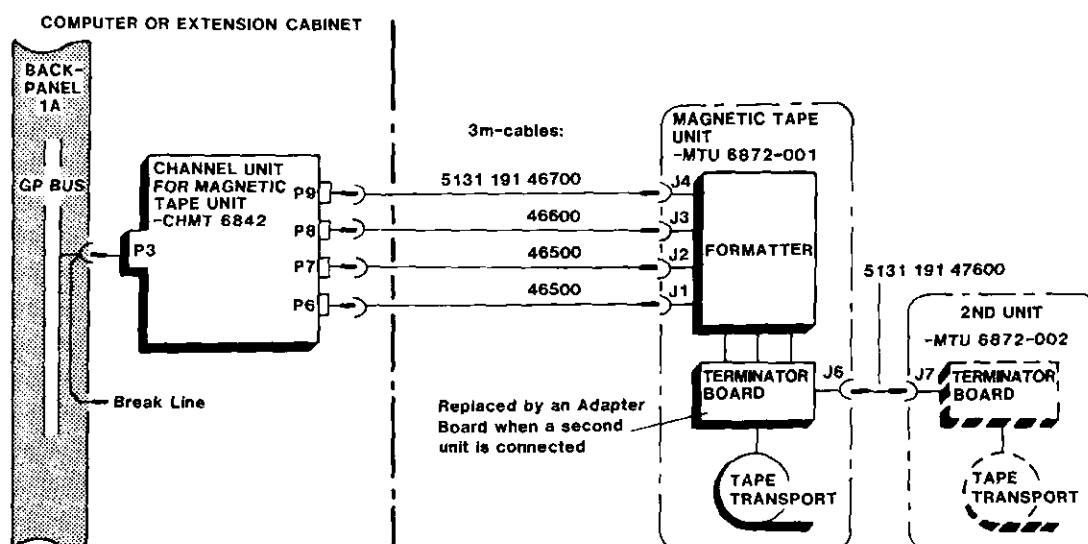


Figure 1.2-11 Connection of Magnetic Tape Unit(s)

### 1.2.5 On-Line Connections

#### General

There are several computer interface units available for communications with a remote data centre, each unit being designed for a specific line configuration and a certain communication procedure. The interface units can be separated in two categories; single-line controllers and multiple-line controllers.

#### Single-Line Controllers

Figure 1.2-12

Four single-line controllers (CHLC 6834-6837) are available as single-board units, connecting to a local modem via a front edge plug. A fifth single-line controller (CHLC 6891) is composed of two parts:

- A line control unit designed in double Eurocard format
- A rack adapter board that enables the line control unit to be plugged into the computers 6810-6814 and 6824.

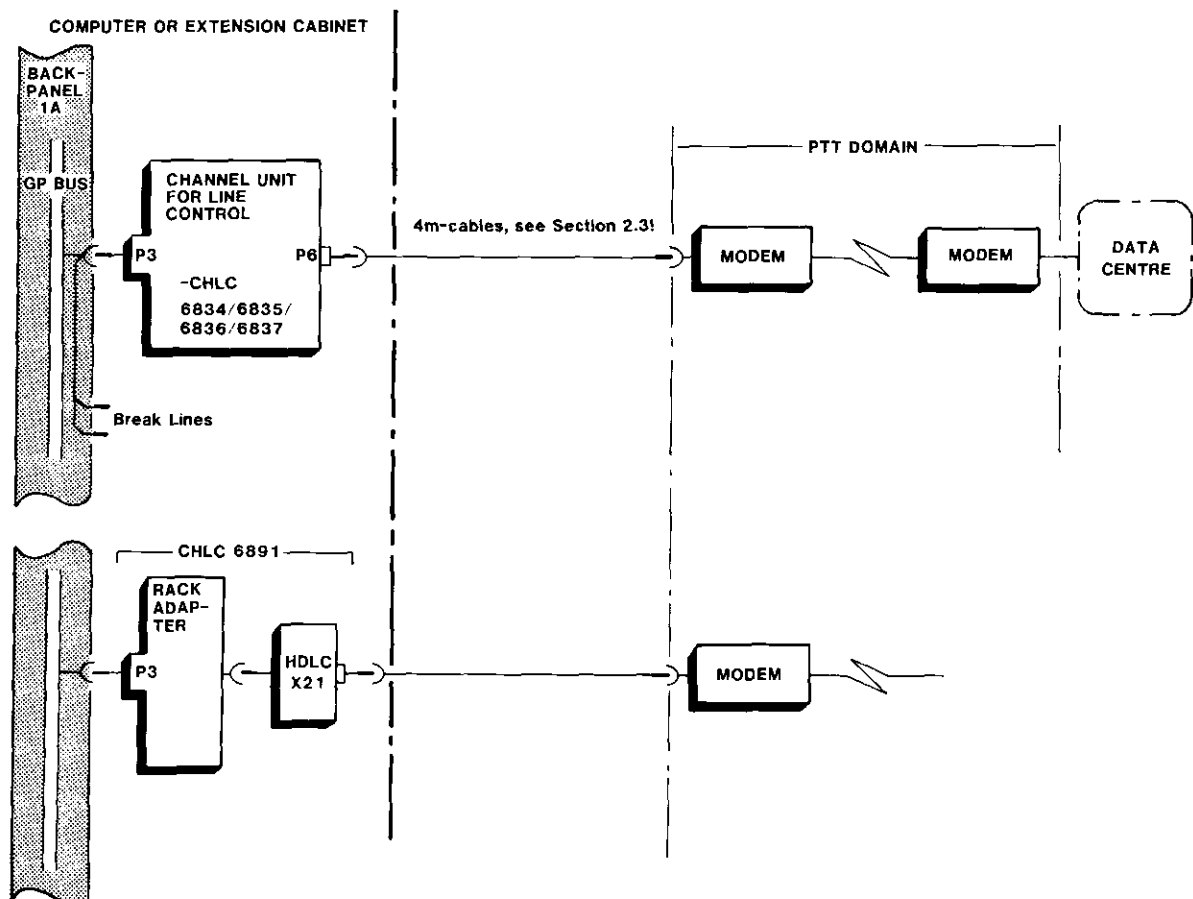


Figure 1.2-12 On-Line Connection via Single-Line Controllers

The main characteristics of the single-line controllers are:

- CHLC 6834, a synchronously operating unit for point to point or multidrop configurations. Line interface: V24/V28. Transfer rate: up to 4.800 bps. Possible procedures: Uniscope 100, BSC, ECMA 16 and others.

- CHLC 6835, a synchronously operating unit for loop configurations. Line interface: V24/V28. Transfer rate: up to 2.400 bps.
- CHLC 6836, a synchronously operating unit for point to point or multidrop configurations. Line interface: V24/V28. Transfer rate: up to 80.000 bps. Possible procedures: HDLC and SDLC.
- CHLC 6837, a synchronously operating unit for loop configurations. Line interface: V24/V28. Transfer rate: up to 4.800 bps. This unit is designed for a specific procedure known as the 'SHB Loop'.
- CHLC 6891, a synchronously operating unit for point to point or multidrop configurations. Line interface: X21/X24/X27. Transfer rate: up to 9.600 bps. Procedure: HDLC.

## Multiple-Line Controllers

Figure 1.2-13

There are two multiple-line controllers available (CHLC 6838/39), both being able to control two lines. However, in ordinary terminal computer applications there is usually just one line used.

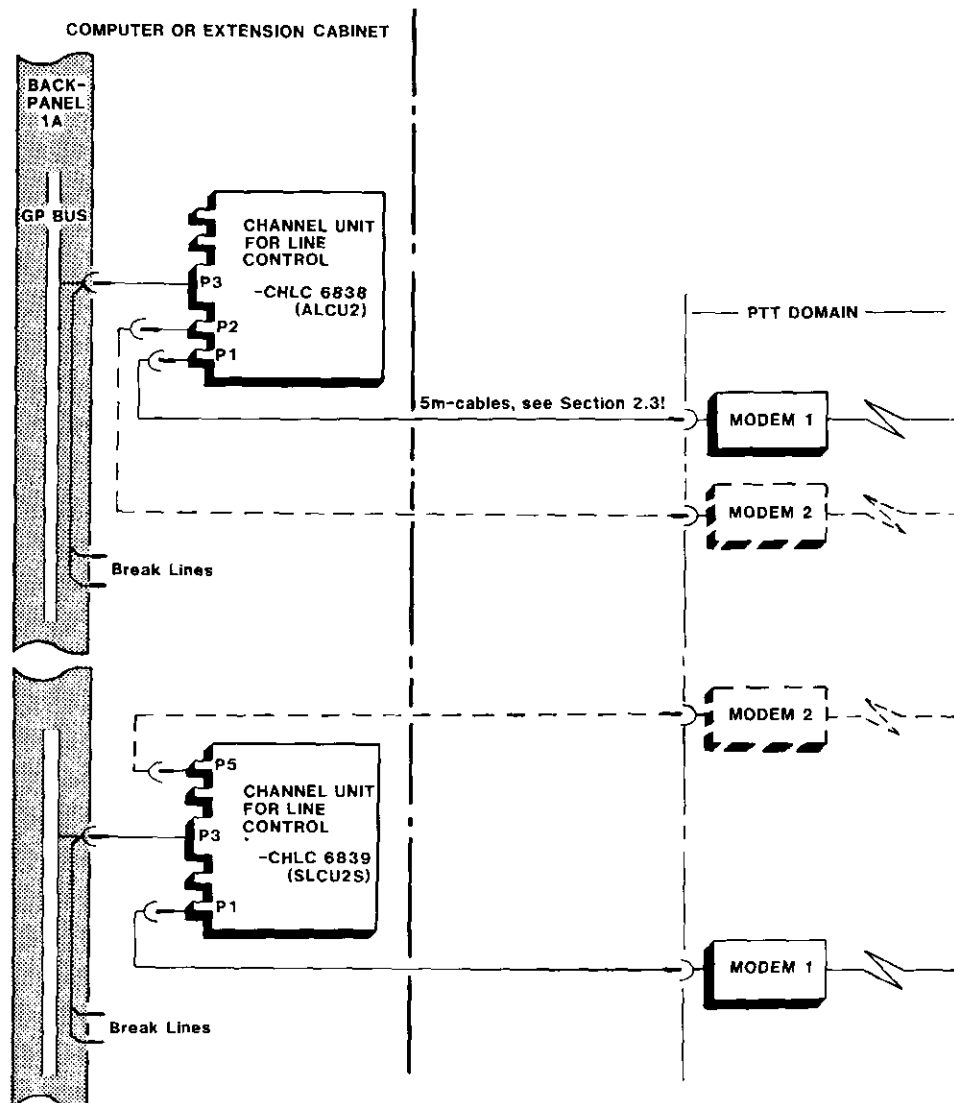
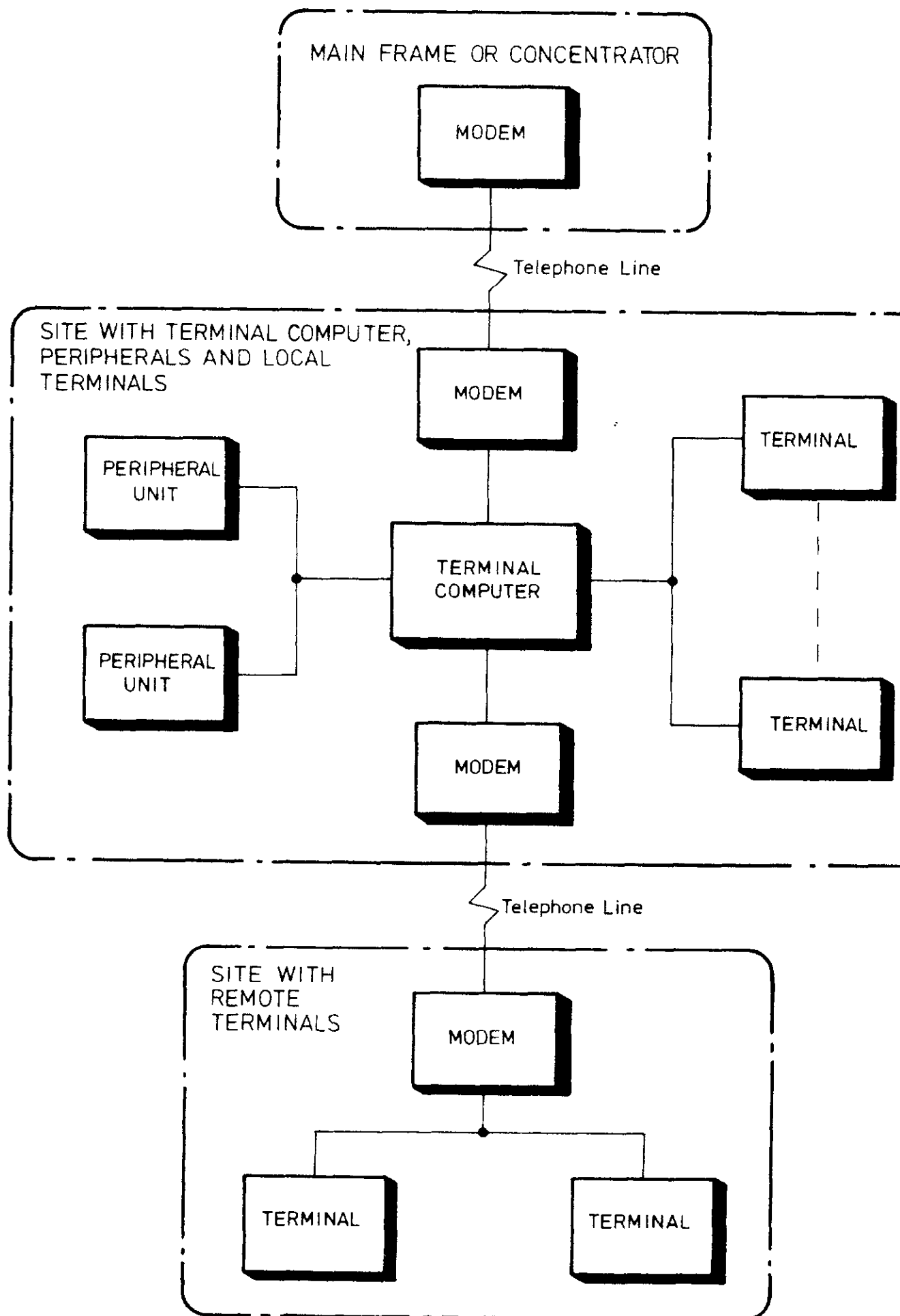


Figure 1.2-13 On-Line Connection via Multiple-Line Controllers

The local modems are connected via cables that are fitted with sockets, fixed to the rack for accepting the rear edge connectors of the controllers.

The main characteristics of the multiple-line controllers are:

- CHLC 6838, Asynchronous Medium Speed Line Control Unit (ALCU2). Line interface: V24. Transfer rate: up to 9.600 bps.
- CHLC 6839, Synchronous Line Control Unit (SLCU2S). Line interface: V24. Transfer rate: up to 9.600 bps.

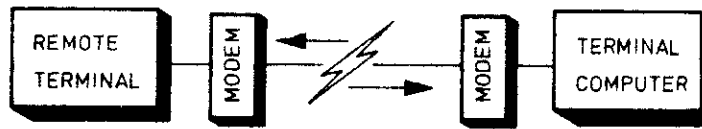




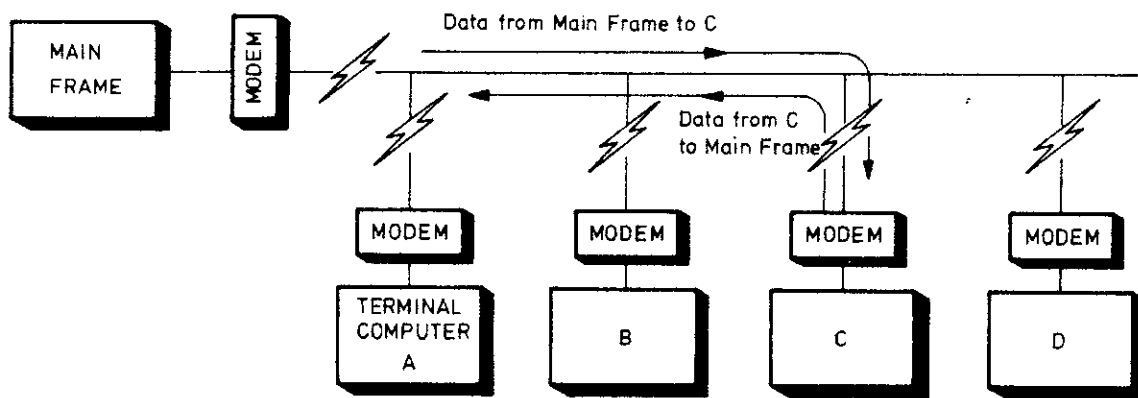


## TYPES OF ON-LINE NETWORKS

POINT TO POINT



MULTIDROP



LOOP

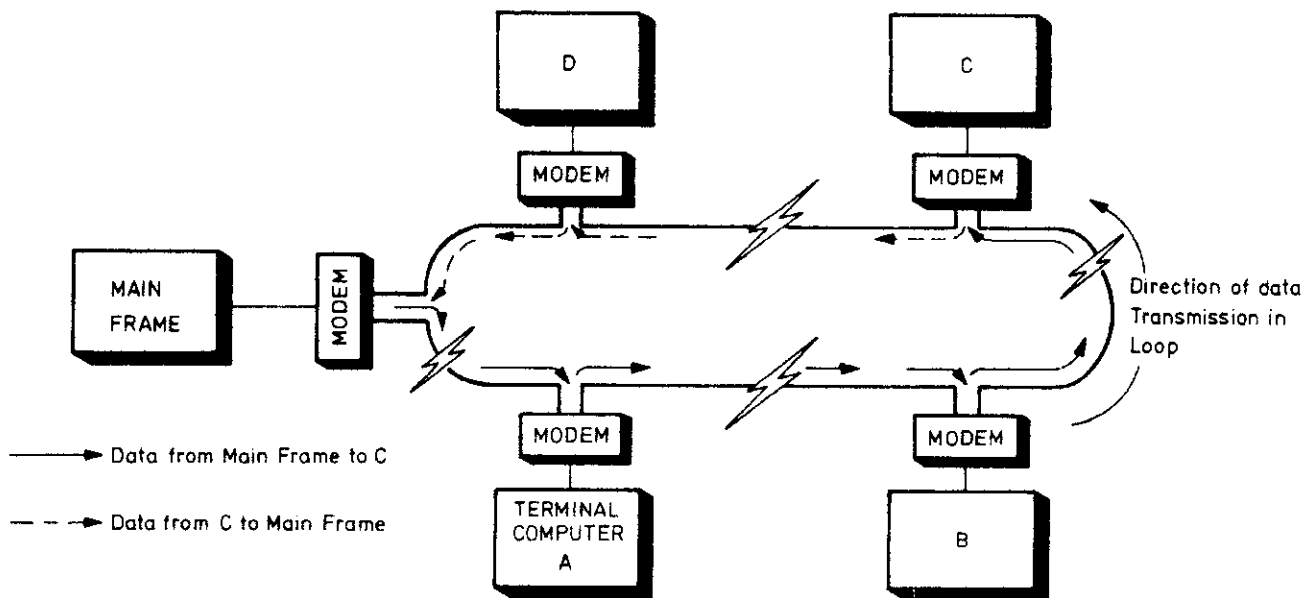


Figure 1.2-14 Basic Configuration and On-Line Networks



## **1.3 BASIC DATA TRANSMISSION TECHNOLOGY**

### **1.3.1 Networks**

#### **Introduction**

Modern data processing technics allow more data to be processed nowadays than was previously possible. To meet the requirement of transferring larger quantities of data faster the Public Data Network is added to the Public Telephone Network which is usually used for data transmission.

#### **Public Telephone Network**

Data transmitted over the Public Telephone Network is converted into analogue signals by means of modem and in the receiving end converted back to digital signals by another modem.

The maximum permissible transfer rate at present is 2400 bps using the 'switched' Public Telephone Network.

Using 'leased' telephone circuits it may be possible to attain rates upto 9600 bps and may be increased further on leased wideband circuits.

#### **Public Data Network**

The Public Data Network is designed for data transmission only. The network is a digital network providing synchronous data transmission, but it is possible to connect asynchronous data terminal equipment for lower transmission rate; 600 - 19.200 bps.

Data terminal equipment with CCITT X21 (X21 bis/X20 bis) interface may be connected to the network.

### **1.3.2 Transfer Techniques**

#### **HDLC Procedure (Protocol)**

HDLC (High-level Data Link Control) is the procedure used in data communication